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LOW INPUT VOLTAGE D.C. TO D.C. CONVERTER

REPORT NUMBER 1

N64-27876 (ACCESSION NUMBER)	(THRU)
62 (PAGES)	1 (CODE)
CR-56451 (NASA CR OR TMX OR AD NUMBER)	06 (CATEGORY)

FACILITY FORM 602

Contract Number NAS 5-3441

National Aeronautics and Space Administration

62 p.

First Tertiary Progress Report

26 June 1963 to 26 September 1963

Goddard Space Flight Center

Greenbelt, Maryland

Submitted by

Minneapolis-Honeywell Regulator Company

ORDNANCE DIVISION

Hopkins, Minnesota

Serial Number 68104

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LOW INPUT VOLTAGE D.C. TO D.C. CONVERTER

REPORT NUMBER I

Contract Number NAS 5-3441

National Aeronautics and Space Administration

First Tertiary Progress Report

26 June 1963 to 26 September 1963

Object: The object of this contract is to design and develop an efficient, reliable low voltage D.C. to high voltage D.C. regulated converter using germanium power transistor switching elements. This converter will be used to convert the low voltage levels of newly developed energy sources to useful higher levels.

Prepared by

John T. Lingle - Project Engineer

Submitted by

Minneapolis-Honeywell Regulator Company
ORDNANCE DIVISION
Hopkins, Minnesota

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SECTION I

PURPOSE

The purpose of this contract is to design and to develop an efficient, reliable, and lightweight, low voltage d. c. to high voltage d. c. regulated converter, using germanium transistors as the power switching element. The converter will be designed to convert the output of thermionic diodes, thermoelectric generators, fuel cells, solar cells, and high performance, single cell electrochemical batteries to a regulated 28 volt d. c. output. The program includes circuit configuration selection, optimization, and new design efforts to reduce losses, size and weight. Effort will be directed toward construction of a breadboard model to verify that the design goals and performance requirements have been optimized.

SECTION II

SUMMARY

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During this first three month period the converter and regulator have been designed, components procured, and a breadboard constructed. The results of work in progress on a related program has provided valuable information which has determined the more favorable voltage regulator approach to be pursued on this project. The "add-on" pulse width modulation voltage regulator has been chosen in place of pulse width modulation of the converter rectification circuit. The reasons for this choice are covered in detail in this report.

Preliminary breadboard tests have shown that the regulated converter efficiency design goal (at least 70% efficiency) has been met for most of the operating conditions. The results show that the converter efficiency ranged between 75 per cent and 82 per cent and the regulator efficiency was over 90 percent for most of the operating range. These results have been encouraging, and effort must now be directed toward improving this performance, simplifying the circuit, and reducing the size and weight of the components. Effort must be directed toward determining the optimum operating frequency of both the converter and the regulator. The current feed-back converter drive circuit is presently being modified so that the operating frequency will be directly proportional to the input voltage.

The results show that voltage regulation is small for load variations but some change occurs with input voltage fluctuations. It will be necessary to compensate the regulator for input voltage changes with a resistor network.

The initial results of this program have been encouraging, and it is now necessary to determine the "trade offs" between size, weight, efficiency, and performance. Further development work will be directed toward simplifying the design to improve reliability and to reduce weight. Environmental testing will be necessary to verify that the design approach meets all requirements.

Author

Some valuable information on the performance characteristics of a single-cell fuel cell and a low input voltage converter has been obtained from a related project. These performance data will be useful on this project and are included in Appendix "A".

SECTION III

CONFERENCES

On July 17, 1963, a conference was held at the NASA - Goddard Space Flight Center, Greenbelt, Maryland to discuss the technical details of this program. Mr. F. C. Yagerhofer, Mr. E. Pasciutti; and Mr. L. J. Veiliette represented NASA, and Mr. B. C. Tierney, Mr. J. T. Lingle, Mr. J. J. Griffis, Mr. J. Torrance, and Mr. G. Anderson represented Honeywell. The development program was outlined, and the converter approach was discussed. The converter drive and synchronizing circuit and the voltage regulation approach were covered in detail. Transistor parameter measurements and transformer construction were elaborated upon. The advantages and disadvantages of transistors and Silicon Controlled Rectifiers for pulse width modulation circuits were reviewed. It was concluded that this program should tend towards a developmental effort as opposed to a strict hardware effort.

SECTION IV

PROJECT DETAILS

A. PARTS PROCUREMENT

During this initial period the circuit approach has been laid out and magnetic components have been designed. The parts necessary to construct the initial breadboard have been ordered and received, including transformer cores and transistors. Furthermore, other components for future needs have been ordered. This includes an order for two MHT 2101 low saturation resistance 150 ampere transistors, which may have a relatively long lead time.

B. CIRCUIT DESIGN

Circuit design effort has been directed toward design of the basic converter circuit and the regulator circuit. This effort has been concentrated on circuit configuration, component selection, and magnetic component design.

1. Basic Converter Circuit Configuration

The Basic Converter Block Diagram is shown in Figure 1. The converter consists of a starting oscillator, to start the circuit under all conditions; a current feedback power oscillator, to chop and transform the low voltage, high current d. c. power to high voltage square wave; a rectification circuit to change this to high voltage d. c.; and a filter.

The converter circuit diagram is shown in Figure 2. The voltage feedback starting oscillator consists of transformers T_1, T_2, transistors Q_1, Q_2, and resistors R_1, R_2, and R_3. Positive feedback from the output transformer T_2 is coupled to the saturating feedback transformer through resistor R_1. This feedback is inductively coupled to the bases of transistors Q_1 and Q_2 to switch one "on" and back bias the other "off". When transformer T_1 saturates the induced feedback,

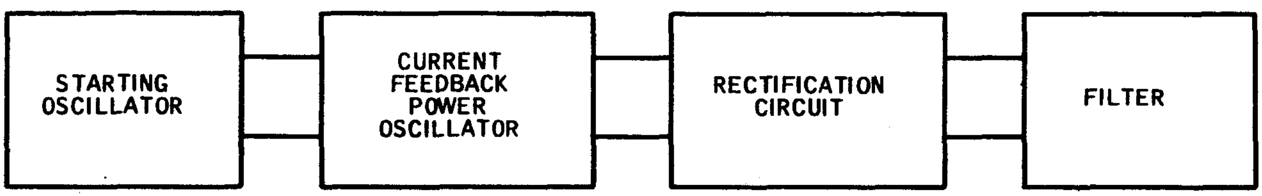

Figure 1 - CONVERTER BLOCK DIAGRAM

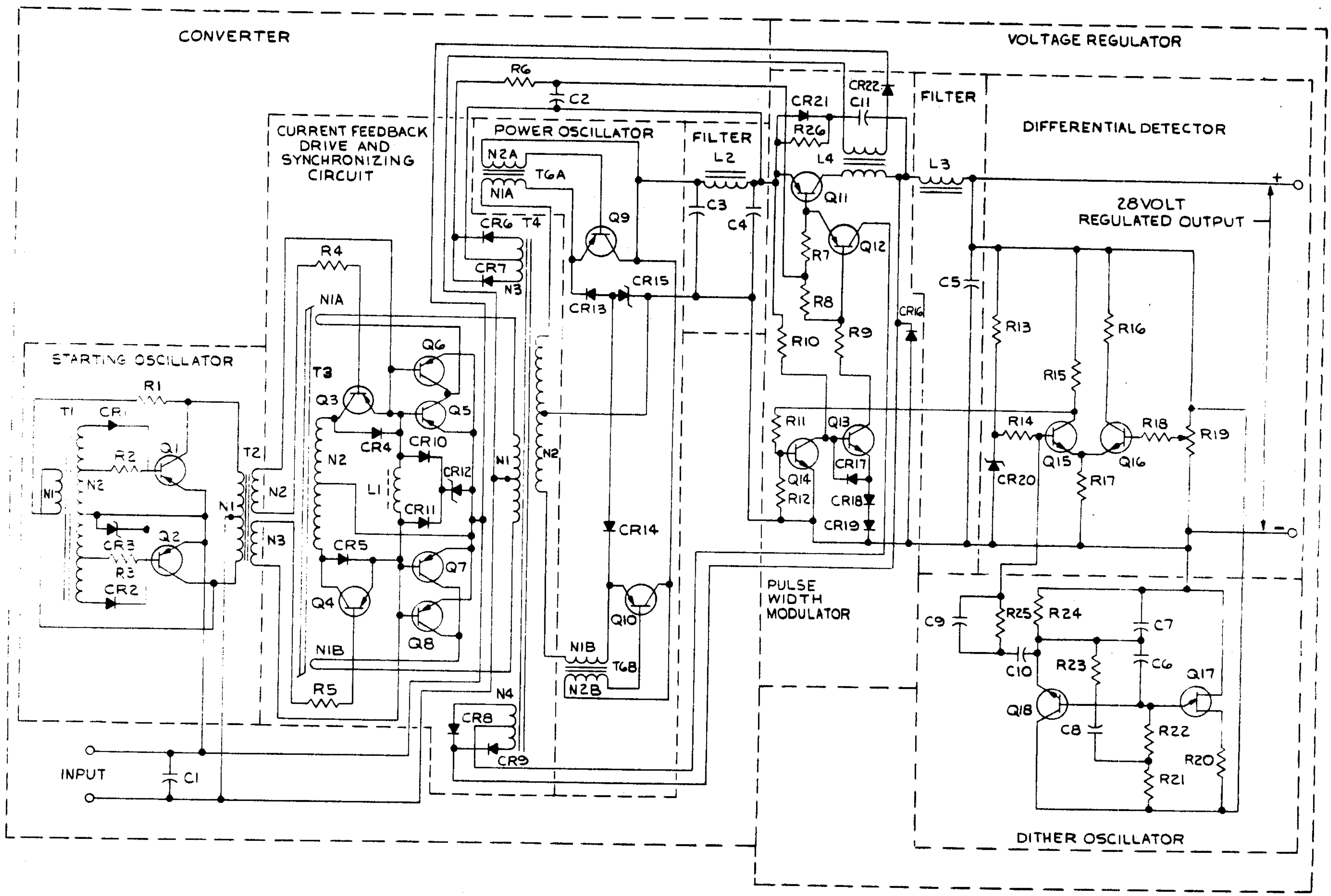

Figure 2 - CONVERTER CIRCUIT DIAGRAM

voltage rapidly declines because resistor R_1 limits the current. This voltage drop reduces the oscillator loop gain to less than unity causing the oscillator to switch. The collapse of transformer leakage flux reverses the feedback signal, turning the formerly non-conducting transistor "on" and back-biasing the opposite transistor "off". Positive feedback maintains operation for the duration of the next half cycle. A zener diode clamp circuit, (CR_1, CR_2, and CR_3 on T_1 winding N_2) maintains constant oscillator frequency by clamping the induced feedback voltage to a constant value. Because the voltage time integral of the transformer core is fixed, the oscillator frequency will be held constant by clamping the induced voltage. The starting oscillator output is coupled to the current feedback power oscillator through T_2 windings N_2 and N_3. This signal starts the power oscillator under all conditions and synchronizes it at a constant frequency.

The power oscillator efficiently chops the low voltage, high current d. c. and transforms it to a higher voltage. The circuit consists of transistors Q_3, Q_4, (Q_5, Q_6) and (Q_7, Q_8); transformers T_3, T_4; reactor L_1; resistors R_4, R_5; and diodes CR_4 through CR_{12}. The power oscillator is a self-excited, current feedback oscillator which is synchronized by the starting oscillator. Current drive, proportional to load, is used to insure that optimum drive is supplied for all load and input voltage conditions. This kind of drive provides maximum efficiency over the load, temperature, and voltage ranges because it is sufficient and optimum to operate the transistors in the low loss saturation region under all conditions. This drive has an advantage over voltage feedback drive which would be designed for the most severe condition and would result in excessive drive losses for other conditions (particularly light load conditions).

When power is applied, current flows through one parallel set of push-pull power transistors (Q_5, Q_6, or Q_7, Q_8), through winding N_1 on T_3, and then through the power transformer T_4 primary N_1 to the negative line. Positive current feedback, proportional to load, is coupled inductively through current feedback transformer T_3 winding N_2 and through either transistor Q_3 or Q_4 to the bases of the parallel switching transistors (Q_5, Q_6 and Q_7, Q_8). This drives one transistor pair into conduction and back biases the opposite pair. Transistors Q_3 and Q_4 in the power oscillator drive current path are used to synchronize the power oscillator at the controlled starting oscillator frequency. Transformer T_2 windings N_2 and N_3 are coupled through resistors R_4 and R_5 to the emitter base junctions of transistors Q_3 and Q_4, respectively.

Thus, the snychronizing oscillator alternately turns one "on" while back biasing the other "off". This arrangement opens the current feedback drive circuit of the conducting power oscillator transistors, causing them to switch "off ". At the same time, the base circuit of the opposite power oscillator transistors is rendered conductive, and the power oscillator switches in synchronism with the starting oscillator. The energy stored in leakage inductance and positive feedback back biases the non-conducting transistors through either diode CR_4 or CR_5.

An important feature of this circuit is that the back biased power oscillator transistors are not directly coupled to the current feedback winding N_2 of T_3 but are coupled through diodes CR_4 or CR_5 when back biased. This feature allows the "off" transistors to be back biased to a higher voltage which will switch them "off " more rapidly. Reactor L_1 is connected across the bases of the push-pull power oscillator transistors. The resetting of its flux during the switching interval provides a large back bias voltage pulse to rapidly switch the formerly conducting transistors "off." The magnitude of the back bias pulse is limited by a clamp consisting of diodes CR_{10}, CR_{11} and zener diode CR_{12}. The stepped-up square wave power from the transformer T_4 secondary winding N_2 is applied to the rectification circuit.

The rectification circuit can consist of either silicon rectifiers or germanium transistors connected as rectifiers. Driven germanium transistors used as rectifiers have an advantage in low output voltage high current applications because the forward drop of the transistor is much less than that of conventional silicon rectifiers. This arrangement decreases losses and improves overall efficiency in suitable applications. The transistor rectification circuit consists of transistors Q_9 and Q_{10} and drive windings N2A and N2B on current transformer T_6. The transistors are biased with respect to the collector. This bias arrangement allows them to be back biased with respect to the collector (which serves as an emitter) in the inverted mode of operation. One of the limitations in the use of transistors as rectifiers is the emitter-to-collector and the emitter-to-base voltage ratings. A zener diode clamp circuit consisting of diodes CR_{13}, CR_{14}, and zener CR_{15} is connected to the emitter circuit to suppress transients which might approach the transistor maximum voltage ratings. Results have shown that transistor rectifiers have an insufficient safety margin for the voltages encountered in this program, and hence the transistor rectification circuit has been replaced by silicon rectifiers.

2. Voltage Regulator

Figure 3 shows the voltage regulator block diagram. The regulator consists of a transistor chopper, which can efficiently chop and pulse width modulate the unregulated d. c. power. The chopped d. c. output then passes through a filter circuit which smooths the pulse power to the desired regulated d. c. voltage. The output voltage is sampled and compared with a zener diode reference by the differential detector circuit. The resulting amplified error signal is applied to a snap-acting trigger amplifier which switches the chopping power transistor, to pulse width modulate the d. c. power effectively and to close the servo control loop. A sawtooth ramp generator supplies a dither signal to the differential detector circuit to control uniformly the frequency of the pulse width modulation circuit.

The right side of Figure 2 shows the voltage regulator circuit. The converter rectified output is passed through a filter consisting of C_3, L_2, and C_4, providing smooth unregulated d. c. power to the pulse width modulation regulator. The main function of this filter is to isolate the converter from the pulse width modulator. This isolation prevents pulse width modulator noise from being fed back onto the input line. Also, the converter power transistors conduct a uniform amount of current during each half cycle for the entire half and this maximizes the converter efficiency.

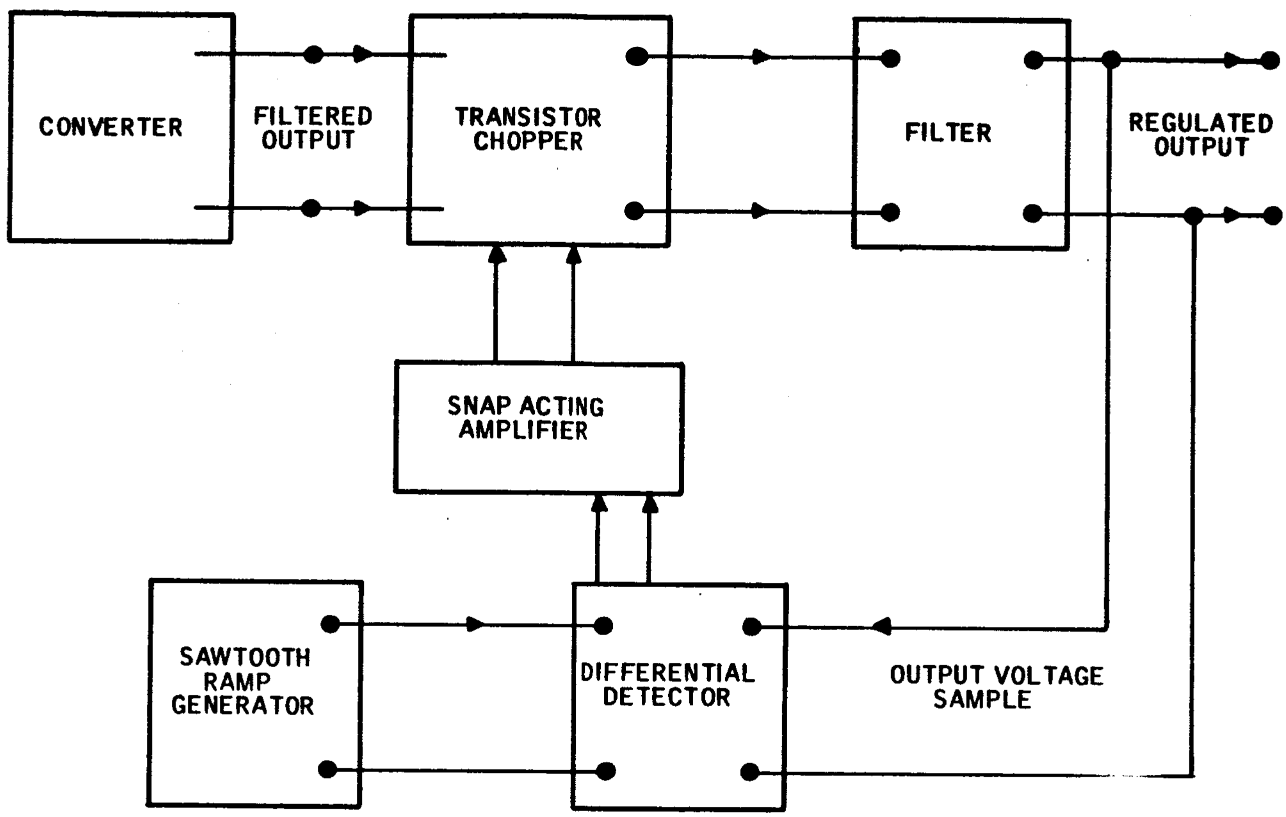

Figure 3 - VOLTAGE REGULATOR BLOCK DIAGRAM

Transistor Q_{11} chops the d. c. current to effectively pulse width modulate the flow of power to the output filter. The output filter consisting of L_3, CR_{16}, and C_5 effectively smooths the pulse power to regulated d. c. To minimize power dissipation in the chopping transistor during switching, a small choke, L_4, has been placed in series with Q_{11}. The operating characteristics of this circuit are such that when switching "on," the transistor must conduct all of the L_3 choke current before it can take over from the free-wheeling diode, CR_{16}, and begin raising the choke terminal voltage. The transistor must conduct the entire load current before its emitter-to-collector voltage can drop to zero. This characteristic causes high instantaneous transistor switching dissipation.

To reduce this switching loss, choke coil L_4 is placed in the transistor collector circuit to absorb an appreciable percentage of the instantaneous voltage drop when the transistor is initially switched into conduction. During this interval the choke voltage drop $e = -L \frac{di}{dt}$ will be large because of the rapid current increase. This reduces the transistor voltage drop considerably during this interval, and a quantity of energy is stored in the choke coil in place of being dissipated in the transistor. The stored energy can be fed back onto the input line during the resetting period. The inductance of this choke is small, and hence it has little effect upon the quiesent portion of the conducting half cycle because the current rate of change is small.

During the switching "off" interval the transistor network must carry the choke current until the transistor emitter-to-collector voltage rises to the maximum "off" condition value. To minimize this dissipation, a network consisting of CR_{21}, C_{11}, and R_{26} is connected across the chopping transistor Q_{11}. When Q_{11} begins to switch "off," a quantity of the choke current is by-passed through CR_{21} and C_{11}. This by-passing reduces the transistor instantaneous dissipation because the collector current is reduced by the amount by-passed through C_{11}. Resistor R_{26} is provided to discharge C_{11}. This mechanism reduces the transistor dissipation by storing some of the high instantaneous power during the switching "off" interval in C_{11}, and dissipating this power in R_{26} during the conduction interval. A more detailed discussion of these effects in switching regulators can be found in the literature. (*)

Breadboard experiments have shown that incorporating choke L_4 does improve efficiency and reduces the chopping transistor temperature. Incorporating the diode capacitor network (CR_{21}, C_{11}, and R_{26}) has not shown any significant change in efficiency. However, improvement in the Ic versus V_{CE} switching wave form trace has been noted. The efficiency does not change significantly when the diode capacitor network is incorporated, because it merely transfers the dissipation from the transistor to the resistor. Since the diode capacitor network has not shown significant efficiency improvement it will be eliminated.

3. Differential Detector and Pulse Width Modulator Operation

The regulator output voltage is sampled by a potentiometer R_{19} across the output. This output voltage sample is applied through R_{18} to one side of the differential detector at the base of Q_{16}. The other side of the differential detector is connected to a zener diode reference through resistor R_{14}. If the output voltage rises so that the voltage sample applied to the base of Q_{16} exceeds the reference voltage at the base of Q_{15}, then a positive amplified error signal will appear at the collector of Q_{15}. This positive error signal is applied through R_{11} to the base of amplifier transistor Q_{14} and will tend to switch it into conduction. Q_{14} is normally held off by resistor R_{12} and requires a positive signal above a threshold value to cause it to conduct. When Q14 conducts, the voltage at the base of Q_{13} declines to 1.0 volt due to current flow through R_{10}. Since the emitter of Q_{13} is biased to plus 1.4 volts by diodes CR_{18} and CR_{19}, transistor Q_{13} will be back biased "off," removing the forward base drive from Q_{12} which is then back biased "off." A positive bias voltage higher than the converter output is provided by a small bias winding (T_4, N_3), rectifiers (CR_6, CR_7) and filter (R_6, C_2). This

*Considerations in the Design of Switching Type Regulators, Russel D. Loucks, Solid State Design, pp. 30-34, April 1963.

bias winding applies a positive voltage source to back bias both Q_{11} and Q_{12} through resistors R_7 and R_8, respectively. The base of the regulator chopping transistor Q_{11} is connected directly to the emitter of Q_{12} and thus Q_{11} is back biased "off" when Q_{12} is back biased. Note that the differential detector output controls the chopping transistor through a network of three amplifying transistors. The resulting high gain insures rapid switching under all load conditions.

4. Regulator Operation

When the converter initially begins operation from a below normal voltage source or from a slowly rising voltage source, the converter output voltage rises and a positive voltage is applied through resistor R_{10} to the base of Q_{13} turning it "on". This voltage causes both transistors Q_{12} and Q_{11} to conduct heavily so that power can pass through to the output circuit. With a low output voltage the error signal will be too low to initiate the chopping regulator, and it will remain fully conducting. This conduction will insure maximum output voltage for a low source voltage and heavy load conditions. As the output voltage rises toward the required value, the output voltage sample will approach that of the zener diode reference CR_{20}. When this feedback voltage sample exceeds the reference, the amplified error signal will switch the three stage amplifier and will rapidly shut "off" the chopping transistor Q_{11}. This action will stop power flow to the output filter and the output voltage will commence declining. A slight output voltage decline will be sensed by the differential detector and it will reverse the error signal to rapidly switch the chopping transistor back into conduction. Thus, the differential detector will cause the regulator to pulse width modulate, and the operating frequency and period will depend upon the load and the filter time constant. To get a more uniform regulator operating frequency a dither oscillator has been used.

The dither oscillator consists of a liner unijunction sawtooth generator. The unijunction relaxation oscillator fires when capacitors C_6 and C_7 become charged with enough voltage to fire Q_{17}. The relaxation oscillator output is applied to the base of an emitter follower consisting of Q_{18} and R_{24}. A boot strap arrangement consisting of R_{21}, R_{22}, R_{23}, C_8, and C_6 is incorporated in this sawtooth generator to give a very linear sawtooth ramp for uniform operation of the switching regulator. More detailed information on this circuit can be found in the literature. (*) The linear sawtooth output of the dither oscillator is applied to the base of differential detector transistor, Q_{15}, through a coupling circuit consisting of C_9, C_{10}, and R_{25}. This R-C coupling circuit shapes the sawtooth wave so that it has a very sharp spike on the leading edge. This sharp spike tends to operate the chopping regulator at a uniform frequency as the output voltage rises to the point where the regulator begins to initiate pulse width modulation. The linear ramp behind the spike tends to space uniformly the duration of the chopping transistor "off" time. The length of this "off" time will depend upon the magnitude of the ramp signal and the magnitude of the error signal. The differential detector will switch when the sum of reference and ramp signals equal the output voltage sample. Thus, circuit operation and pulse duration time depend upon a coincidence in the ramp signal and output voltage sample magnitudes.

C. REGULATION METHODS

The following two methods of pulse width modulation regulation have been considered:

(1) Pulse width modulation of the converter rectification circuit

(2) An add-on pulse width modulation regulator connected after the converter output filter.

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* General Electric Transistor Manual, Sixth Edition, Pg. 96

1. Pulse Width Modulation of the Rectification Circuit

Voltage regulation by pulse width modulation of the converter rectification circuit has been investigated under a current Signal Corps contract. (*) The results of this work have shown that satisfactory voltage regulation can be obtained by this method; however, the efficiency obtained was lower than expected. Investigation of this regulation method has revealed the following difficulties.

- Pulse width modulation of the rectification circuit introduced large ripple on the input line.
- High converter input ripple made accurate input power measurements difficult.
- The driven transistors used as rectifiers were subjected to higher emitter-to-collector voltages than anticipated.
- Investigation has shown that the converter transformer core loss increased when pulse width modulation regulation was introduced into the rectification circuit.

A power source with high d. c. impedance contributed to high input line ripple. With a high source impedance, the converter input voltage rises considerably at no load or light load. Pulse width modulation initially delays the rectification circuit conduction, and the converter operates at light load for the initial portion of each half cycle. Thus, during this portion of each half cycle the source voltage rises to a high value. After the delay interval, the rectification circuit is gated

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* "Low Input Voltage Conversion" DA 36-039-SC-90808, U. S. Army Electronics Research and Development Laboratory

"on" and the source voltage declines to the loaded value. The relatively high impedance of some of the new energy sources will cause high ripple on the input line when pulse width modulation is introduced in this manner. Also, the collapse of primary leakage flux during the switching interval will tend to feed energy back into the power source.

This feedback increases the input ripple voltage. Ripple induced in this way will be especially large if the source impedance is high. The input line ripple is very difficult to filter because the currents are very high and because large amounts of energy are stored in the input lead inductance and in leakage inductances. If the source impedance is lower, the input ripple voltage will be less, but the input ripple current will be increased. It has been concluded that pulse width modulation of the rectification circuit increases input line ripple because there is no effective filter between the pulse width modulator and the input line.

Pulse width modulation of the rectification circuit hindered accurate measurement of the input power because of the a. c. ripple component superimposed upon the d. c. ripple. Because the a. c. current component tended to lag its voltage by appropriately 90°, the a. c. component prevented accurate calculation of true input power by mere multiplication of the average voltmeter reading times the average ammeter reading. With this high input ripple, it was necessary to plot the input voltage and current wave forms, to multiply the instantaneous values together, and to integrate to obtain the true input power. This method is tedious and the accuracy is questionable.

The net effect of regulation by pulse width modulation of the rectification circuit was to induce the transformer voltage waveforms shown in Figure 4. Figure 4A shows the waveform without pulse width modulation, and Figure 4B shows the effect of pulse width modulation of the rectification circuit. These transformer waveforms show that the induced voltage rises to a high value when the rectification

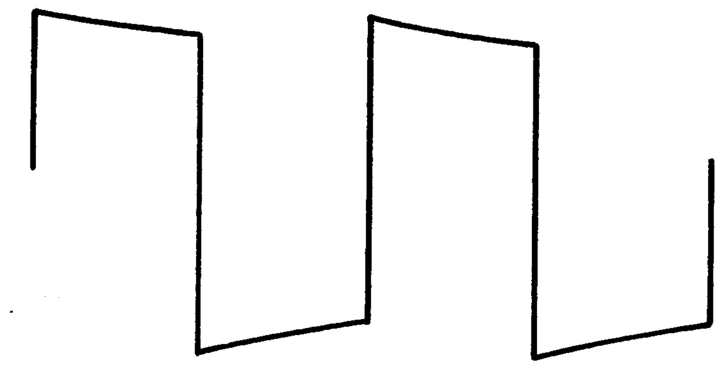

Figure 4A - TRANSFORMER WAVEFORM WITHOUT PULSE WIDTH MODULATION OF THE RECTIFICATION CIRCUIT

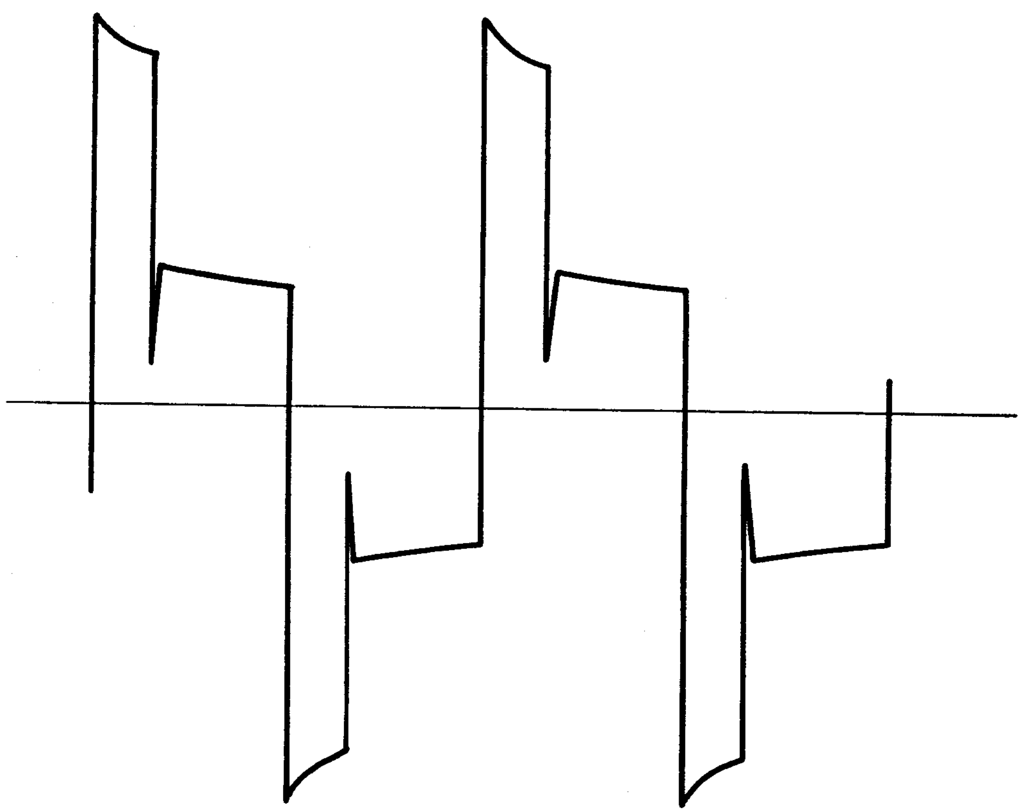

Figure 4B - WITH PULSE WIDTH MODULATOR OF THE RECTIFICATION CIRCUIT

Figure 4 - TRANSFORMER INDUCED VOLTAGE WAVEFORMS

transistor is held "off" during the initial portion of each half cycle. This impresses a high forward voltage across the transistor which is to be gated "on" and a high inverse voltage across the transistor which is back biased in the inverted mode. This voltage is especially high when a source having high impedance is used. Secondary leakage inductance can cause voltage transients which subject the transistors to higher voltage spikes. Because of the high, impressed voltage, it is necessary to use transistors with collector-to-emitter, and emitter-to-base voltage ratings of 100 volts or more. The choice of transistors with the required parameters is limited.

By comparing Figure 4A with Figure 4B it can be noted that the voltage time integral of Figure 4B is much larger per half cycle. Thus, pulse width modulation of the rectification circuit increased the maximum operating core flux density and hence increased transformer core losses.

Pulse width modulation of the rectification circuit decreased the basic converter efficiency. The core losses were increased as noted above. Also, higher peak currents, flowing through the transistors and transformer windings for a smaller portion of each half cycle, increased converter losses. Input current pulses of larger magnitude were necessary to achieve the same output power when pulse width modulation was used. Transformer I^2R losses and transistor losses increased because of the higher instantaneous currents carried. Thus, the converter section would instantaneously operate at a much higher load to achieve a given output power, depending upon the pulse width during that half cycle. Furthermore, the operating converter no-load losses must be provided during the gate interval when it does not send power to the load.

2. <u>Switching Characteristics of the Power Transistors When Pulse Width Modulation of the Rectification Circuit is Incorporated</u>

Figure 5 shows the converter power oscillator transistor voltage and current wave forms when regulation is accomplished by pulse width modulation of the rectification circuit.

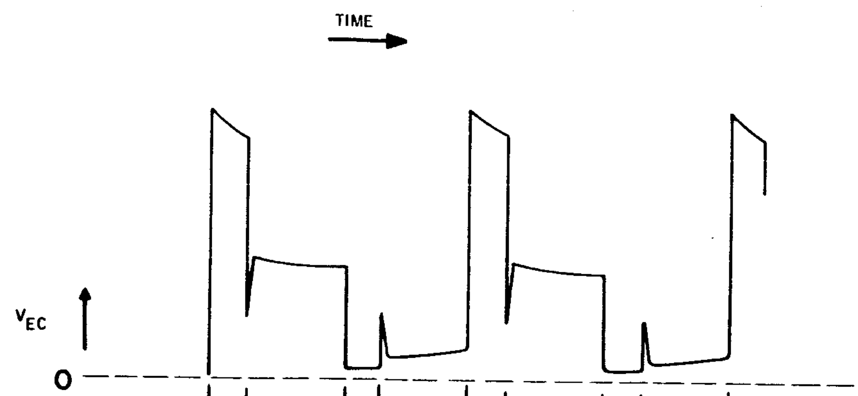

Figure 5A - VOLTAGE WAVEFORM (Ved) ACROSS THE POWER OSCILLATOR TRANSISTOR WHEN REGULATION IS ACCOMPLISHED BY PULSE WIDTH MODULATION OF THE RECTIFICATION CIRCUIT

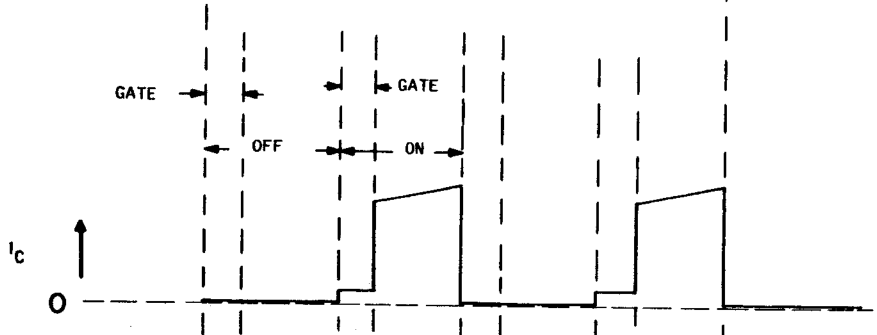

Figure 5B - CORRESPONDING COLLECTOR CURRENT WAVEFORMS

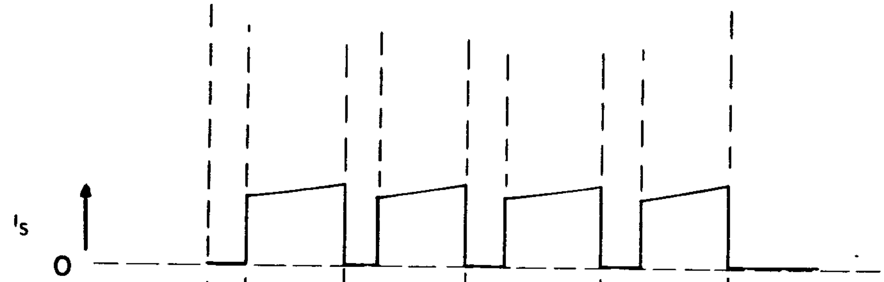

Figure 5C - RECTIFICATION CIRCUIT OUTPUT CURRENT

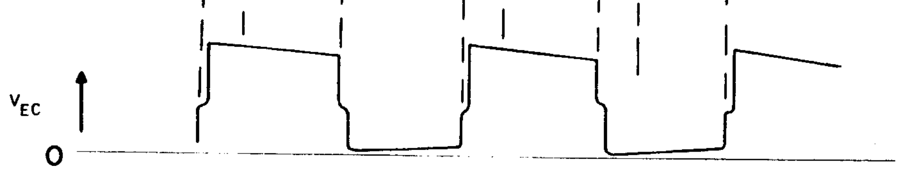

Figure 5D - TRANSISTOR VOLTAGE WAVEFORMS VEC WITHOUT PULSE WIDTH MODULATION OF THE RECTIFICATION CIRCUIT

Figure 5 - OSCILLATOR WAVEFORMS

Examination of Figure 5A shows that when the transistor switches "off" the voltage rises to a very high value and remains high for the duration of the pulse delay gate. This initial high voltage portion of the cycle represents the rectification transistor non-conductive period. The rectification circuit output is shown on Figure 5C. The converter is not supplying load to the output filter and does not draw current heavily from the supply during this interval as shown by Figures 5B and 5C. This instantaneous light load reduces the power source IR drops, causing its terminal voltage to rise. This is impressed upon the converter causing it to instantaneously operate from a higher voltage source during the initial delay gate portion of each half cycle. During this interval the transformer induced voltage is much higher as indicated by the Figure 5A voltage wave form across the "off" transistor. When the rectification transistor is allowed to conduct after the delay interval the induced voltage in the transformer will decline very rapidly to a lower value due to the sudden load place upon the converter. This transient loading is shown in Figure 5B.

Note that the transformer induced voltage drops to a very low value for an appreciable period during this transient loading condition. Apparently, the transistor is incapable of picking up the load immediately because the conducting transistor has a sudden saturation voltage increase during this interval. After a short interval, the increased current feedback will again drive the conducting transistor back into the low saturation region, lowering the saturation voltage to approximately 50 millivolts. This cycle is shown on the right side of Figure 5A, which represents the transistor in the conducting region.

After the transient loading interval, the voltage across the non-conducting transistor will assume a nearly constant value determined by source voltage, which is dependent upon load and source characteristics. Note that with the particular source used,an appreciable change in transformer-induced voltage occurred between the "off" and "on" conditions of the rectification circuit. Naturally, this type of voltage wave form increases the power transformer core loss. This type of wave form also increases the power oscillator transistor switching loss, when switching from the conducting to the "off" state, because higher "off" voltages are encountered. The transient loading effects which cause the transistor to come out of saturation during transient loading also increase transistor dissipation. Thus, the full advantage of initially switching "on" at light load is not fully realized because additional losses are caused by transient loading. Pulse width modulation of the rectification circuit, however, does diminish transistor dissipation which can be caused by a period of zero, or very low, transformer induced voltage. This phenomenon is illustrated in Figure 5D. This waveform shows the transistor characteristics without pulse width modulation of the rectification circuit. Note the delay in the transistor switching characteristics approximately half way between the "off" condition and the "on" condition. During this delay, the voltage drop across the transistor is about equal to the supply voltage and the transistor current is large during this interval. This switching pause lasts for an appreciable length of time, depending on load, and causes high transistor dissipation. During this pause, the transformer induced voltage is very nearly zero. This switching delay is caused by the secondary current changing more rapidly than the primary magnetizing current. During this interval the choke input filter tends to draw current through the secondary winding. The winding half that attempts to switch positive is immediately loaded by the heavy choke current. This secondary current is demagnetizing; and if it exceeds the primary ampere turns, it over-powers the primary magnetomotive force, preventing the power transformer core from switching. This effect holds the transformer-induced voltage very near zero until sufficient primary magnetizing current can overcome this. More detailed discussion of this effect can be found in the literature*.

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* Power Transistor Circuitry - Quarterly Report III pp 21-23, and Final Report - J. T. Lingle - Honeywell Ordnance Division, Contract DA-36-39-SC-71161. Lib. of Congress P. B - 143304.

Slow transistor switching also contributes to pauses during the switching interval. The switching "off" transistor collector current does not immediately decline, and the switching "on" transistor cannot immediately pick up the load current. During this interval, both transistors may be conducting and their respective magnetomotive forces cancel each other. If this occurs, the switching "on" transistor collector current must exceed that of the switching "off" transistor, before it can attempt to switch the transformer core. In fact, the magnetomotive force produced by the switching "on" transistor must overcome the magnetomotive force of the switching "off" transistor, as well as the magnetomotive force caused by high choke coil current in the secondary winding half that is attempting to switch positive. Thus, the switching "on" transistor may have to conduct a very high current before the core can be switched. Slow switching "off" of one transistor will cause the switching "on" transistor current to rise to a higher value before switching the core, and this will increase switching time and dissipation. Experiments have shown that this effect can be diminished or practically eliminated by pulse width modulation of the rectification circuit. This modulation will prevent the secondary current from immediately building up to a very high value and will allow the oscillator transistors and the transformer core to switch to the desired position before load current is drawn. This is one of the main advantages of pulse width modulation of the rectification circuit. Experiments have shown that much more rapid switching can be obtained when this pulse width modulation is used. However, the results have not increased the efficiency as much as expected.

Because of characteristics noted above, converter regulation by pulse width modulation of the rectification circuit did not produce efficiencies as high as expected. The efficiencies obtained were in the 50 per cent to 60 per cent range (about 15 per cent less than had been anticipated). Examination of the results showed that the increased losses were widely distributed throughout the circuit as indicated above. These difficulties, combined with high voltages across the rectification transistors when operating in this mode, decreased the desirability of this approach.

3. Pulse Width Modulation With an Add-On Voltage Regulator

Because of the above reasons, voltage regulation effort was directed toward a straight converter circuit with a switching type add-on regulator. With this approach, the converter output filter isolates the voltage conversion and regulation functions, permitting the low input voltage converter to operate at its maximum efficiency. The add-on switching regulator can respond quickly. The converter section operates independently of the regulator, lending the device to modular construction. The regulator can be contained in a separate module or become an optional feature if desired. The add-on regulator can pulse width modulate at a much higher frequency than the converter frequency, and it can utilize high speed germanium or silicon transistors. The transistor voltage requirements are not as severe because they are not subjected to inverse voltages.

Another advantage of the add-on pulse width modulation regulator is that it will introduce less ripple on the input line, and have less effect upon the source. This reducing source ripple might be very important when operating from the newer energy sources such as thermionic diodes, thermo-electric generators, and fuel cells. The add-on regulator will also simplify the instrumentation required to measure the performance of the device. The input power can be measured more accurately by ordinary ammeters and voltmeters because the input ripple will be a small percentage of the total input power. The converter output is filtered before passing to the regulator, and the converter output power alone can be measured easily at this point with standard meters. The output power of the regulated converter can also be easily measured at the output. Thus, measurements can be taken at the converter input, at the converter output, and at the regulator output. This flexibility permits measurement and efficiency calculations for the converter alone, the regulator alone, and the overall system.

Because of the above advantages and disadvantages, an add-on pulse width modulation regulator has been chosen for the initial portion of this program. This choice does not rule out the possibility of using pulse width modulation of the rectification circuit; however, at this time it appears that the add-on regulator has more advantages than the regulator which pulse width modulates the rectification circuit. The primary advantage of the add-on regulator is that the filter between the converter rectification circuit and the chopping regulator will prevent the regulator from interfering with the operation of the converter thereby lowering the basic conversion efficiency. Moreover, the filter between the regulator and the converter will prevent regulator noise from being fed back onto the input line, thus reducing the radio noise and source problems. The possible higher frequency operation of the regulator circuit will also reduce regulator time response, and the filter size and weight. By using a straight converter and an add-on regulator, a choice can be made between a choke input or a capacitor input filter on the converter itself. When pulse width modulation of the rectification circuit was used, a choke input filter was mandatory because the ripple voltage was too high for an input capacitor.

D. RECTIFIER REQUIREMENTS

Examination of the converter operating with a pulse width modulation rectification circuit has shown that high voltages are impressed across the rectifying transistors. These experiments were run with the Signal Corps converter breadboard having a regulated 6.5 volt output. The measurements show that the voltage impressed across the rectifying transistors was very large. For the regulated 6.5 volt output, voltages as high as 30 volts were impressed across the rectifying transistors. Should this scheme be used to achieve a regulated 28 volt output, the voltage across the rectifying transistors might be as high as 100 volts. At the present, it is difficult to obtain satisfactory transistors with collector-to-emitter and emitter-to-base voltage ratings this high. Some transistors can be selected to withstand this voltage, but the design might be marginal if the transistors are operated near their maximum ratings. If voltage spikes occur, the operating conditions may exceed the ratings. Because of this, pulse width modulation of the rectification circuit using transistors does not appear very promising at this time. The use of cilicon controlled rectifiers in this position could be considered; however, these have disadvantage in higher forward voltage drop and high gate power requirements.

Breadboard experiments with an add-on pulse width modulation regulator have shown that the converter output voltage rises considerably depending upon the converter design and the anticipated swing in input voltage and load. For a 6.5 volt regulator output, the converter output voltage was observed to run as high as 24 volts under certain conditions, impressing 48 volts across the rectification transistors. This condition, of course, is satisfactory for a 6.5 volt output, since transistors rated at this voltage can be obtained readily. Experiments have shown that a converter designed to feed into a 28 volt "add-on" pulse width modulation regulator can have an output of over 50 volts under high input voltage - light load conditions if it is designed for wide input voltage swings. This condition would subject the rectifiers to peak inverse voltages of at least 100 volts. Under these operating conditions it is desirable to use silicon rectifiers because the transistor rectification method would be marginal. The rectifier peak inverse voltages will depend upon the output voltage, the input voltage variations, and the load variations expected in a particular system.

Silicon rectifiers appear to be the best choice for a regulated converter having a 28 volt output. The efficiency will be slightly lower because of a higher forward drop, but the required voltage ratings can be obtained. The requirements of the rectifiers and the rectification circuit will be investigated further during the next quarter. At the present, germanium transistors are the only transistors which can be considered as rectifiers because they have relatively high emitter-to-base voltage ratings, much higher than silicon transistors. Of course, at the 28 volt output level the rectifier losses are not as great as they are at the lower output voltages; therefore, the use of silicon rectifiers does not degrade greatly the efficiency characteristics.

E. CONVERTER PERFORMANCE

Performance characteristics of the unregulated converter are shown on Figure 6. The curves show efficiency versus output power for various input voltages. Examination of these data shows that the efficiency ranged between 73 and 82 per cent. At light loads the efficiency is less for higher input voltages. The power transformer flux density increases with input voltage, and this increases core loss and lowers light load efficiency. The curve for a 0.8 volt input shows that efficiencies of 78.5 per cent, 82 per cent, and 75 per cent were obtained for power outputs of 10, 20, and 50 watts, respectively. This efficiency curve begins to droop above 30 watts due to increased primary and secondary current and I^2R losses which are required to achieve the necessary power output with low input voltages. The curves for higher input voltages achieve maximum efficiency at higher power outputs. For example, the curves for 1.0, 1.2, and 1.4 volts achieve maximum efficiencies at 30, 37, and 45 watts, respectively. The maximum point for the 1.6 volt curve is above 50 watts. The slope of the curves indicates that the converter will maintain relatively high efficiencies at loads greater than 50 watts.

It is expected that the converter performance at heavier loads can be improved by redesigning the power transformer. The redesigning of the transformer will be directed toward increasing the secondary wire size at the expense of the primary wire size.

During the initial stages of breadboard checkout, driven transistors were used as rectifiers. This method tended to minimize rectification losses; however, the transistors were subjected to high voltages when operated in the inverted mode. At high input voltages a zener diode clamp was necessary to protect the transistor rectification circuit against voltage spikes. To remedy this situation, the transistor rectification circuit has been replaced by silicon rectifiers. This change

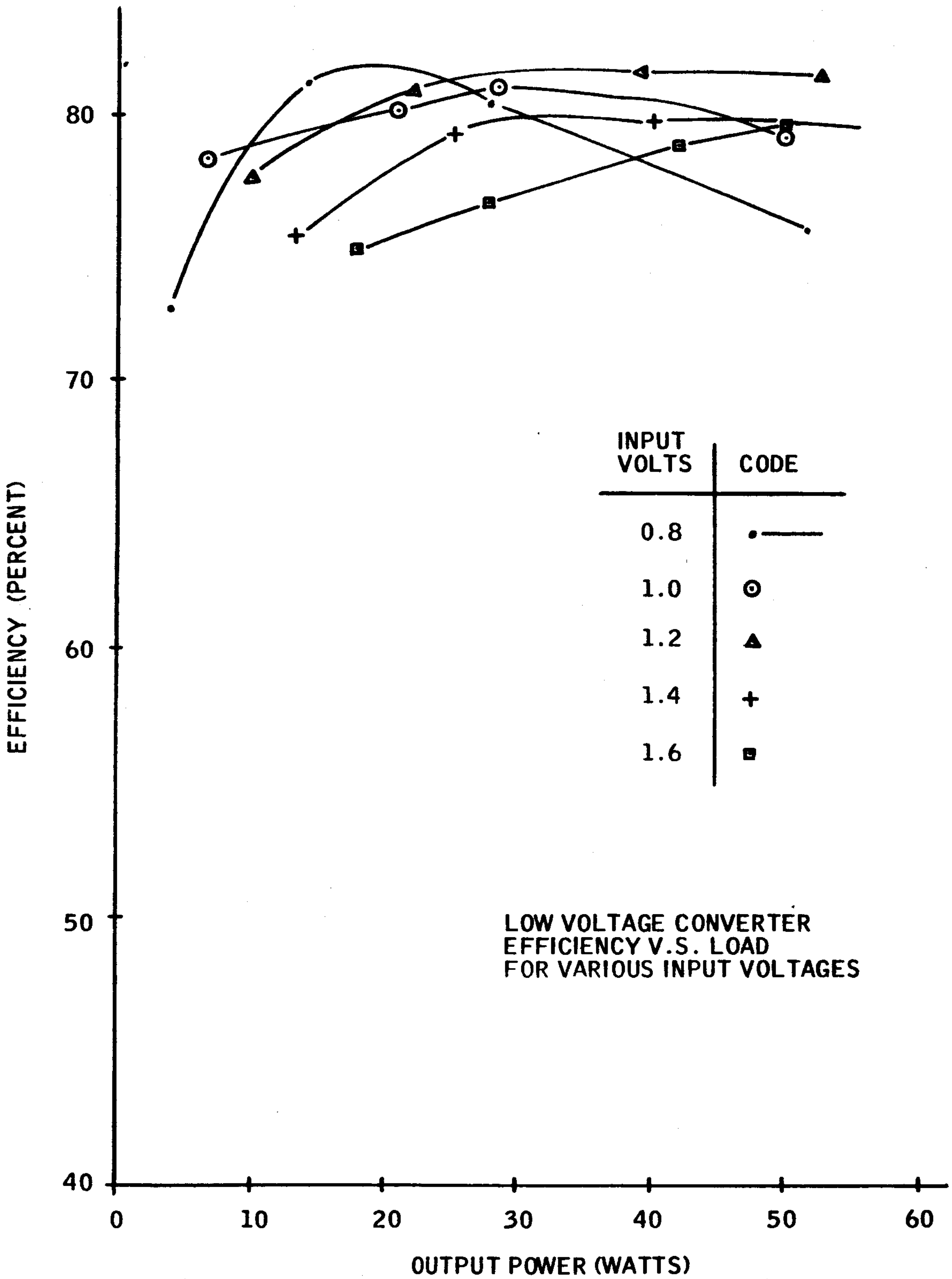

Figure 6 - LOW VOLTAGE CONVERTER EFFICIENCY VERSUS LOAD FOR VARIOUS INPUT VOLTAGES

did not increase the losses by any great extent since rectification losses are a relatively small percentage of the total when the output voltage is 28 volts or higher. Silicon rectifiers were in use when the performance data of Figure 6 were obtained. It was concluded that transistor rectification circuits should be used only on converters having low output voltages.

Initial breadboard checks were directed toward determining the effect of various operating frequencies on converter efficiency. In general, higher operating frequencies tend to lower over-all efficiency. Preliminary curves of efficiency versus load for two frequencies are shown on Figure 7. Circuit parameter changes have since improved the overall efficiency and these data are now obsolete. Nevertheless, the curves can be compared to determine the effect of frequency on efficiency. The curves show the difference between 600 and 800 cps operation at 1.5 volt input. The efficiency increase was between 1.0 per cent and 2.5 per cent when the operating frequency was lowered from 800 cps to 600 cps. Calculations indicate that with the same transformer and operating voltage the core losses will remain nearly constant over the frequency ranges presently being used. Therefore, the decline in efficiency is caused primarily by transistor switching losses. For higher frequency operation it is imperative that switching losses be minimized. For optimum performance with a power source having wide voltage variations, it is desirable to increase the frequency with input voltage to maintain constant flux. Initial data have been obtained with the converter synchronized to a fixed frequency. Frequencies used have been between 400 and 900 cps. The breadboard drive circuit is currently being changed so that the operating frequency will vary proportionally with input voltage. This hookup will tend to maintain the operating flux density constant and prevent saturation of the output transformer at higher input voltages.

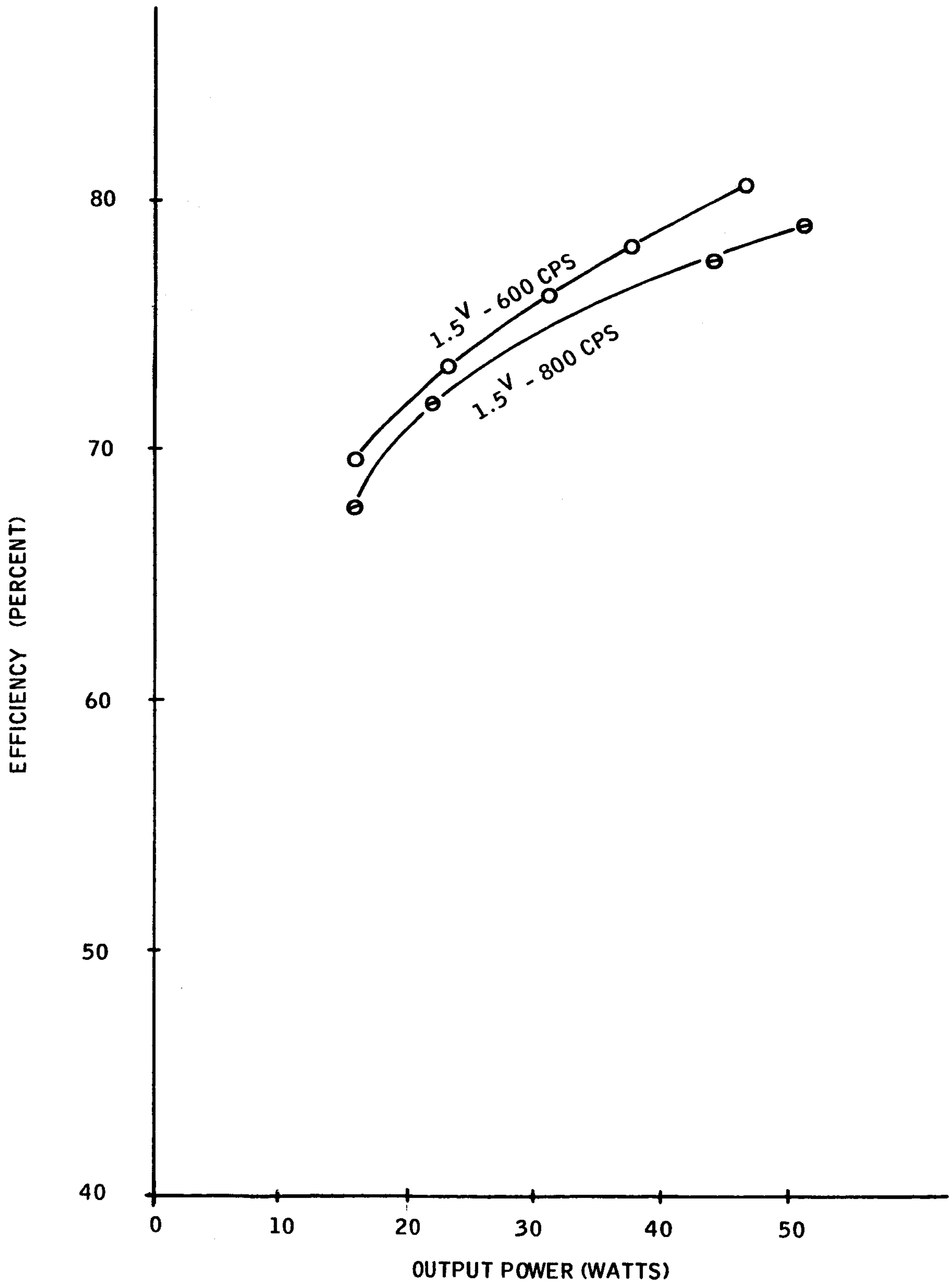

Figure 7 - LOW VOLTAGE CONVERTER EFFICIENCY VERSUS LOAD FOR TWO FREQUENCIES

F. VOLTAGE REGULATOR PERFORMANCE

Preliminary performance data have been obtained on the regulator and on the converter and regulator combined.

1. Regulator Check Out

The add-on pulse width modulation regulator was initially checked out using 65 ampere 2N2731 transistors for the power-switching element. This transistor had very low saturation resistance, but its current capability was much greater than necessary, and the switching speed was somewhat slow. The use of faster chopper and driver transistors improved performance.

An H-200E tetrode and a 2N2832 diffused-base transistor have both been used as the switching element. Efficiency improved as faster switching transistors were used. The H-200E was superior to the 2N2731, and the 2N2832 provided some additional improvement. Efforts are currently being directed toward improved regulator performance. Some higher voltage, high-frequency transistors have been ordered for this application, including both the switching transistor and the driver.

2. Regulator Performance With a Laboratory Power Supply

Figure 8 shows performance data for the 28 volt regulator alone, operating from a laboratory power supply. The curves show regulator efficiency versus load for various input voltages. The dotted curve shows the regulator performance at a 25 volt input, which is too low to require pulse width modulation. With this low input voltage, the switching transistor is maintained fully conducting. The efficiency at this input voltage is above 94 per cent for power outputs between 10 and 50 watts. The regulator performance curves for the 30 volt input also show high

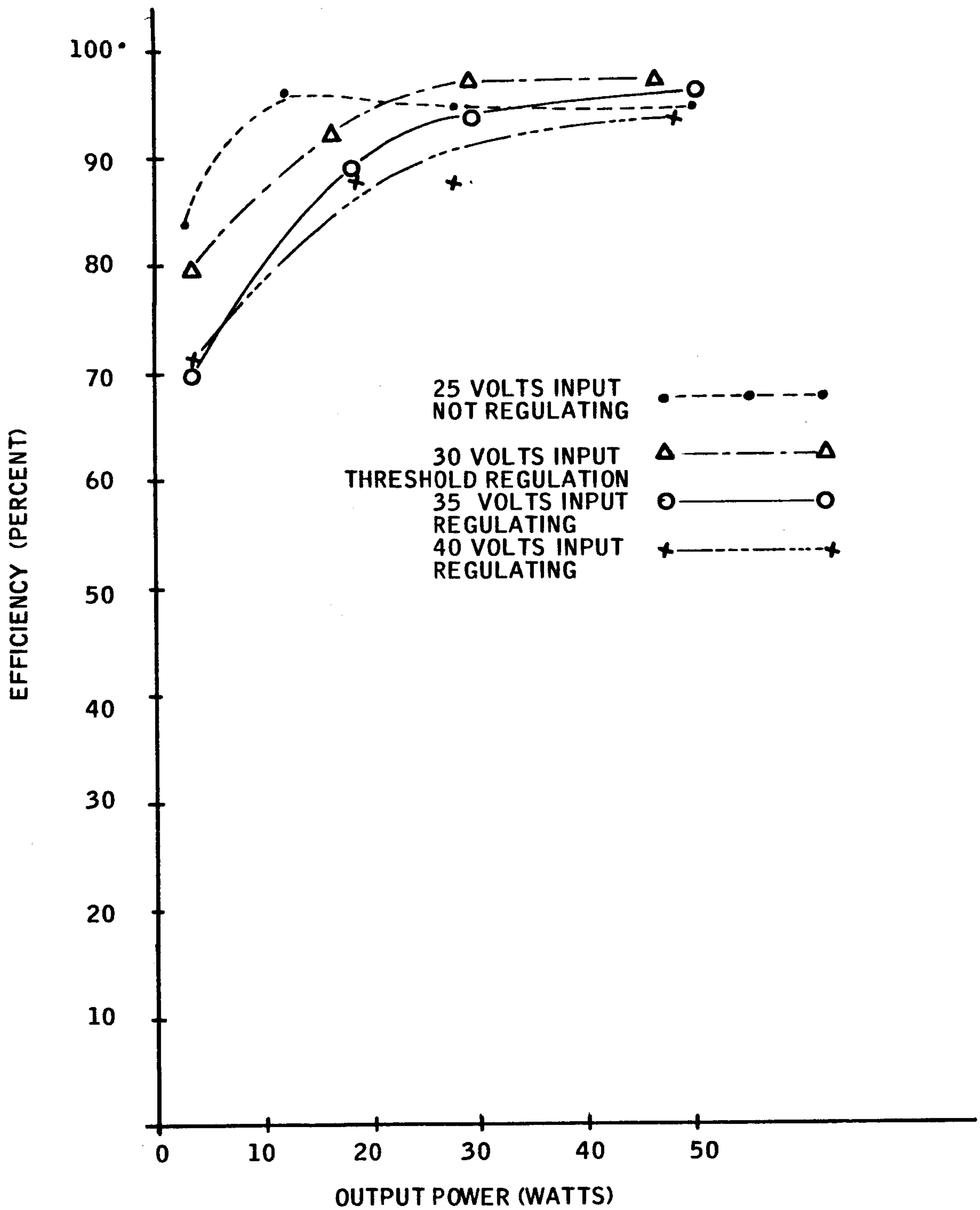

Figure 8 - 28 VOLT PULSE WIDTH MODULATION REGULATOR PERFORMANCE

efficiency, varying from 90 per cent at 14 watts to 97 per cent at 47 watts. This curve represents threshold performance where pulse width modulation is initiated. At this threshold level, the "off" time is a relatively small percentage of the period. The efficiency is somewhat lower at light loads because the "off" time is a greater percentage of the period and the fixed losses are a greater percentage of the input power.

The curves for 35 volt and 40 volt inputs show that the efficiency tends to decline slightly as the input voltage is increased. The efficiency is still high at 50 watts output, being 96 per cent and 93.5 per cent for 35 volt and 40 volt inputs, respectively. The efficiency declines as the input voltage is increased because the "off" time is a greater percentage of the period, the transistor switching losses are increased, the choke core losses are increased, and the free wheeling diode dissipation is increased. Thus, the above regulator performance curves show that the "add-on" 28 volt regulator efficiency is high and declines somewhat as the input voltage is increased. Therefore, it is desireable to minimize input voltage swing and to operate within practical limits to achieve maximum over-all efficiency.

G. REGULATED CONVERTER PERFORMANCE

1. Measured Performance

The regulator was connected to the converter and performance data were measured. The measured, regulated converter performance has been plotted on Figure 9. These curves show overall efficiency versus output power for various input voltages. The maximum efficiencies obtained were 74 per cent, 73.5 per cent, and 71 per cent for the 0.8 volt, 1.0 volt and 1.2 volt inputs, respectively. The

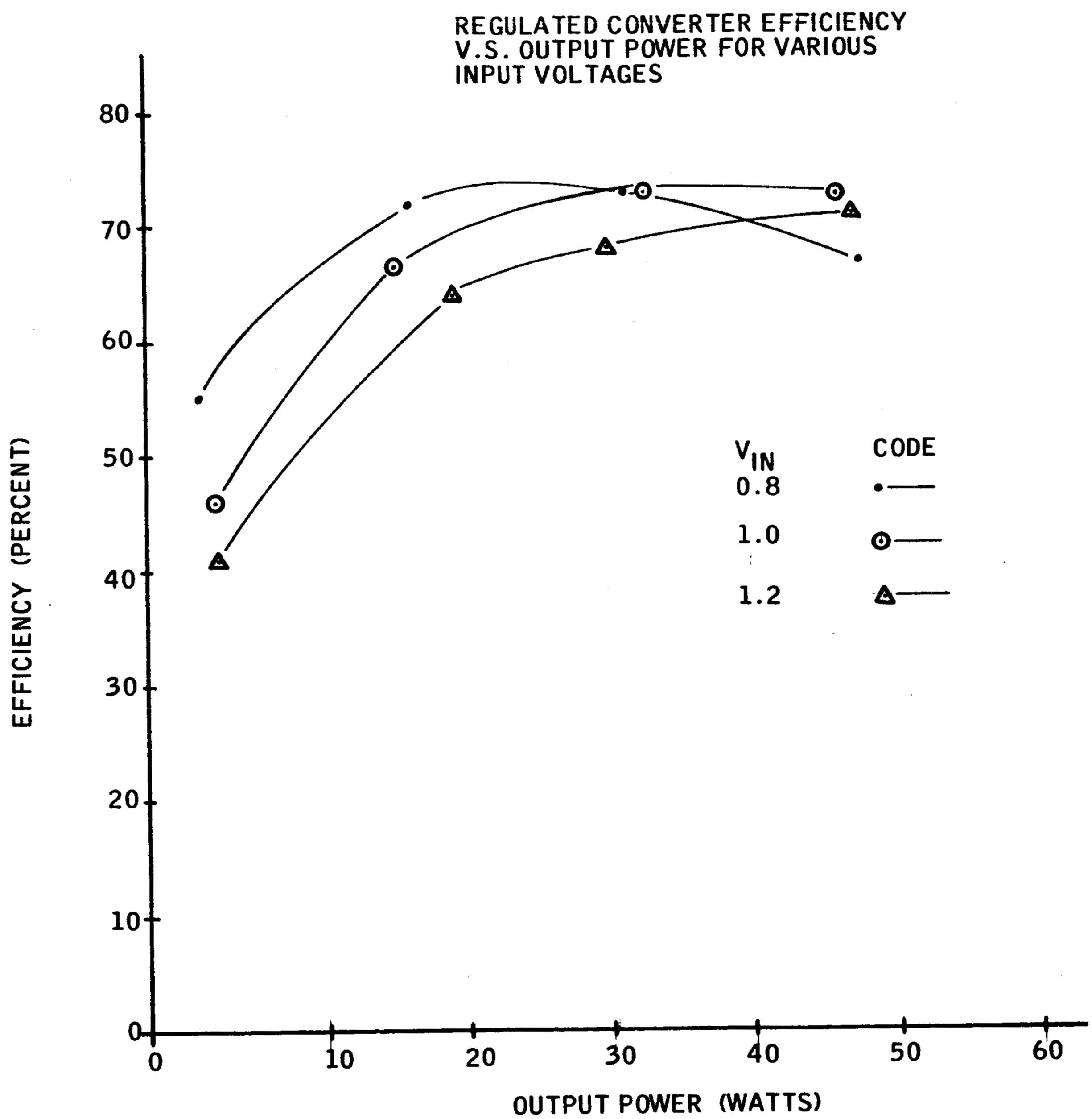

Figure 9 - REGULATED CONVERTER EFFICIENCY VERSUS OUTPUT POWER FOR VARIOUS INPUT VOLTAGES

respective power outputs at maximum efficiency were 26 watts, 38 watts, and 47 watts. These curves show that the regulated converter efficiency design goal (over 70 per cent) was met for the following input voltages and output powers:

0.8 volt input: 14 to 40 watts

1.0 volt input: 20 to 50 watts

1.2 volt input: 36 to 50 watts

As noted above, the light load efficiency declines because fixed losses are a greater percentage of the input power. The efficiency declines with higher input voltages at light load because of the characteristics of the regulator noted above. The voltage dependency of the efficiency characteristics is determined by both the converter and regulator characteristics.

2. Calculated Performance

An anticipated performance curve for a regulated converter was obtained by multiplying points on the unregulated converter curve, Figure 6, by corresponding points on the regulator performance curve of Figure 8. Points for corresponding output powers were obtained for 1.0 volt input converter performance and 40 volt input regulator performance. The calculated performance curve was then plotted on Figure 10. This curve shows that efficiencies between 70 per cent and 75 per cent can be expected for power outputs between 22 and 50 watts for a regulated converter operating from a 1.0 volt input. This calculation is not strictly accurate because it assumes a constant regulator input voltage. This is not the case since the regulator input voltage declines with load. The regulated converter measured performance curve for a 1.0 volt input was also plotted on Figure 10. By comparing the calculated performance curve with the measured performance curve, it can be seen that the difference does not exceed 2 per cent. This is close and well within experimental error considering the number of meter readings involved. These data indicate that there was no appreciable performance degradation when the converter and regulator were coupled together.

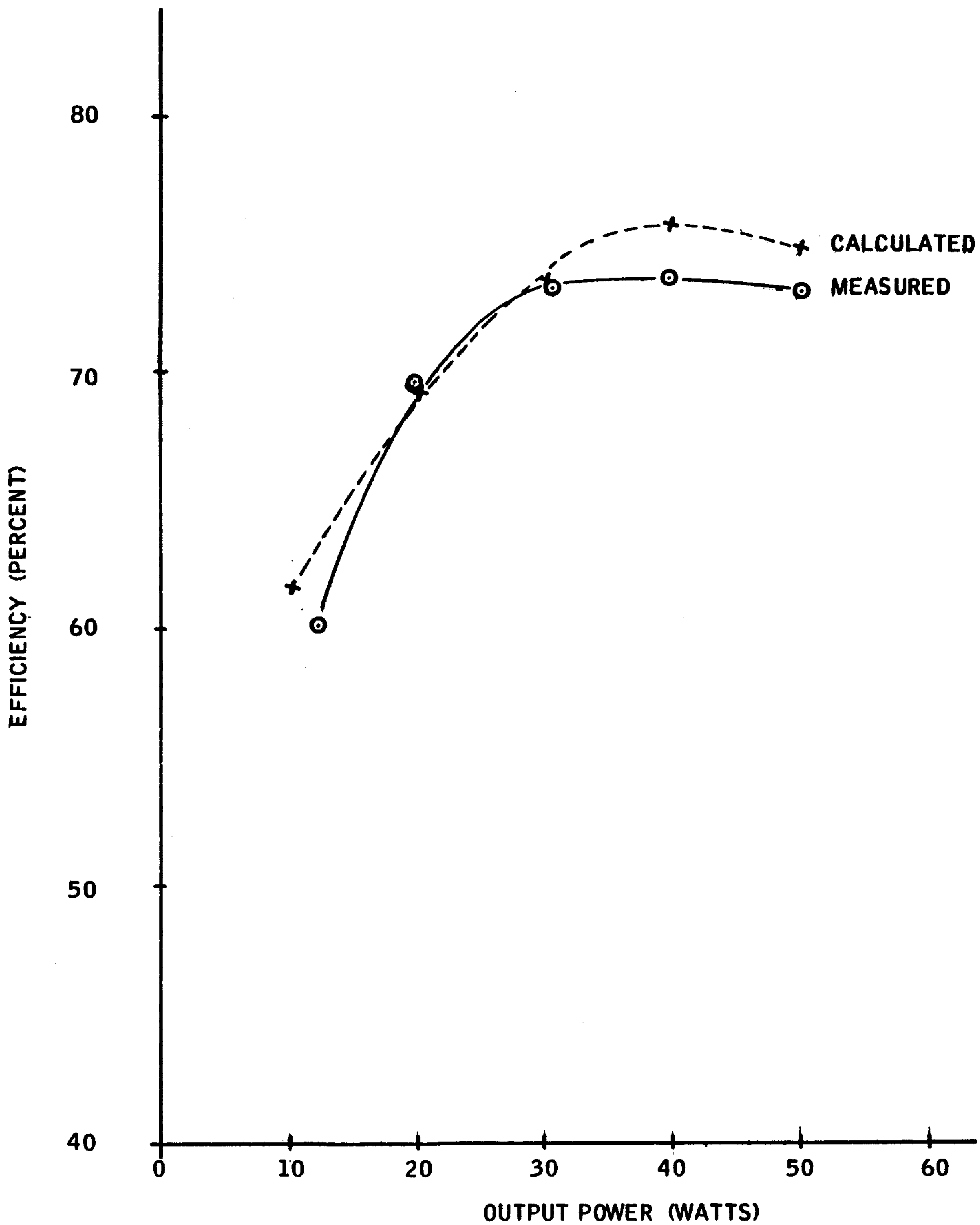

Figure 10 - CALCULATED EFFICIENCY FOR A REGULATOR CONVERTER

3. Voltage Regulation

The regulated converter voltage regulation is shown on Figure 11. This figure shows curves of output voltage versus load for various input voltages. The curves for 1.2 and 1.0 volt inputs were almost flat for load changes. The curve for the 0.8 volt input was reasonably flat at light load but drooped at heavy load. The 0.8 volt curve drooped at heavy load because the regulator input voltage was near the threshold level, and it dropped below the set point at heavy load. Thus, at heavy load the regulator input voltage was too low, and it became inoperative and fully conductive. The output voltage curves are reasonably flat over the load range for all conditions where the regulator is operating. However, there is an appreciable change in output as the input voltage is varied. To give better regulation it will be necessary to compensate for input voltage changes. The initial results show that tight regulation has been obtained over the load range where the regulator is operating. It will be necessary to change the set point to improve performance at the lower 0.8 volt input. The results also indicate that input voltage compensation must be incorporated in the regulator to achieve the desired performance. This compensation can be accomplished by a resistor network, which will be incorporated next quarter.

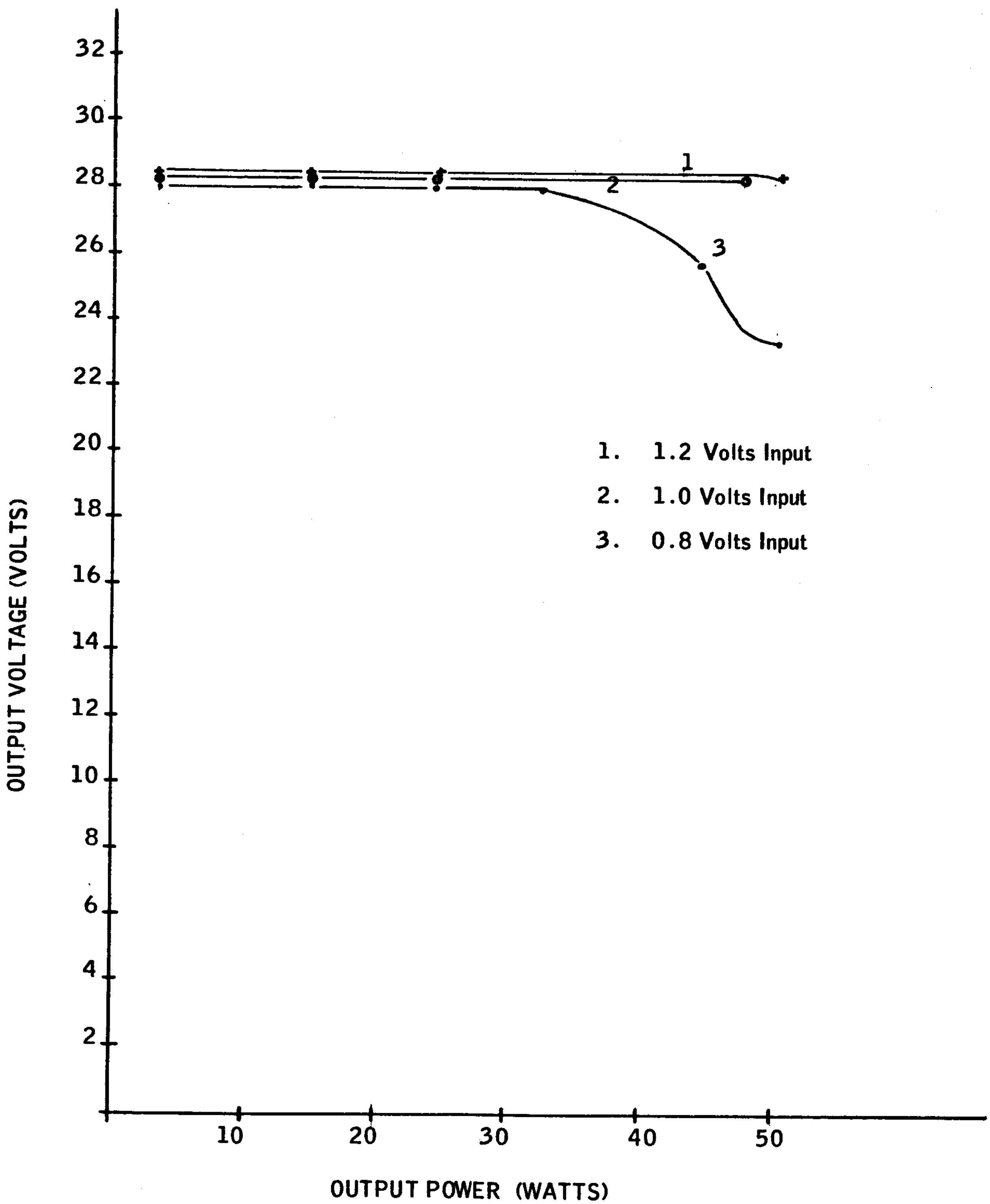

Figure 11 - REGULATED CONVERTER OUTPUT VOLTAGE VERSUS LOAD FOR VARIOUS INPUT VOLTAGE

SECTION V

CONCLUSIONS

Efforts were directed toward the design and fabrication of a regulated low input voltage converter. Initial efforts were concentrated on transformer design and selection of the converter and regulator circuit configuration.

Two types of switching voltage regulators were considered for this application:

1. Voltage regulation by pulse width modulation of the rectification circuit.

2. An "Add-on" pulse width modulation regulator.

The voltage regulator circuit selection was aided by research and development effort currently in progress on a related program. Breadboard operation showed that voltage regulation by pulse width modulation gave the following disadvantages:

1. Input line ripple was increased.
2. Transistor switching losses and saturation losses were increased.
3. Power transformer core losses and I^2R losses were increased.
4. Rectification transistors were subjected to higher voltages than anticipated.
5. The regulated converter efficiency was lower than expected due to the losses noted above.

These disadvantages outweighed the advantages of using the rectification circuit as both a rectifier and a regulator. Because of the above results it was concluded that the initial efforts of this program should be directed toward a converter with an "add-on" pulse width modulation regulator. This converter and regulator breadboard was constructed and operated. The converter efficiency ranged between 75 percent and 82 percent over most of the input voltage and output power ranges under consideration. The regulator efficiency was above 90 percent over most of the operating ranges considered. The regulated converter efficiency met the design goal (over 70 per cent) for the following input voltage and load conditions;

0.8 volt input - 14 to 40 watts output
1.0 volt input - 20 to 50 watts output
1.2 volt input - 36 to 50 watts output

Initial regulator operation has shown that although voltage regulation is tight for load variations, it requires some additional compensation for input voltage changes. The initial results have been promising since regulation approaches the design requirements. Improvement will be directed toward compensating the regulator for input voltage changes.

Experiments have shown that driven transistors used as rectifiers are subjected to very high inverse voltages when the output voltage exceeds 28 volts. A converter with a nominal 28 volt output will have much higher output voltages at high input voltage, light load conditions. These high voltages approach the transistor maximum ratings and hence reduce reliability. Experiments have shown that transistor rectifiers increase the efficiency by only a few per cent when used at the 28 volt level. Because of the voltage problem it has been concluded that driven transistor rectification circuits should only be used in applications having maximum output voltages less than 28 volts. Silicon rectifiers are now used for rectification with only a slight decrease in efficiency.

The initial phase of this program has shown results that approach the design goals for circuit performance. Some improvement in circuit performance is still desired; however, the main emphasis must now be placed upon circuit simplification and weight reduction. This emphasis should be directed toward higher frequency operation and lighter components. The initial results have shown that efficiency declines when the frequency increases. Effort is currently being directed at changing the converter drive circuit so that the frequency will change proportionally to input voltage. The operating frequency will increase with input voltage to maintain constant flux density and to prevent saturation of the output transformer. The new drive circuit will still maintain current feed-back, which is essential to high efficiency over wide input voltage and load variations.

Experiments with the "add-on" pulse width modulation voltage regulator have shown that it does not degrade the converter performance when it is incorporated into the system. The converter filter between the power oscillator and the pulse width modulation regulator provides the necessary isolation to prevent interactions. Thus, the "add-on" regulator is superior to regulation by pulse width modulation of the rectification circuit in that it does not degrade the basic converter performance and does not introduce any appreciable amount of ripple on the input line.

SECTION VI

PROGRAM FOR THE NEXT INTERVAL

Research and development work for the next interval will be directed toward improving the device performance, simplifying the drive circuit, and reducing component weights.

The drive circuit will be simplified by removing the fixed frequency synchronizer and replacing it with a circuit to make the operating frequency proportional to input voltage. This change is currently in progress and appears promising.

Efforts will be made to determine the optimum operating frequency range for the converter and for the "add-on" pulse width modulation regulator. Higher operating frequencies may allow reduction in the power transformer weight and size.

The high regulator efficiency may allow an increase in regulator operating frequency, thus reducing the size and weight of regulator filter components.

The use of higher voltage and higher speed transistors in the switching regulator will be investigated further. Both germanium and silicon transistors will be considered for the regulator chopper and its driver. Regulator performance will be improved by incorporating input voltage compensation.

Special effort will be directed towards the design of the power transformer, which is the largest component. Design effort will be directed toward the proper choice of steel, core configuration, and windings to achieve an optimum balance between efficiency and weight.

SECTION VII

IDENTIFICATION OF PERSONNEL

Resumes of the personnel assigned to this program are as follows:

D. A. NELSON, Chief Engineer, Electromechanical Group, Ordnance Division, Minneapolis Operations

Experience

Presently directing development engineering groups for weapon, missile and space systems, as well as their subsystems and components.

Eight years in supervisory and administrative capacities on missile systems and components, structures, fuzing, rockets and special weapons, including:

Assistant Project Manager, ASROC,

Missile System Section Chief,

Special Weapons Development

Naval Ordnance Engineering Officer on ammunition, rocket, and fuzing systems.

Aeronautical Research Scientist with National Advisory Committee for Aeronautics

Member of Engineering Faculty, University of Minnesota

Senior Engineer, A. O. Smith Company

Professional Background

BSME University of Minnesota, 1942
MSME University of Minnesota, 1945

B. C. TIERNEY, Project Supervisor, Power Supplies

Experience

Presently supervising development of power source conditioning and control equipment, including:

Low voltage conversion devices for use with fuel cells, solar arrays, thermonic diodes, and thermoelectric generators.

High performance DC to AC static inverters

On-board electrical power system design for manned, earth orbiting space station

Solid state and gas lasers

Previously supervised environmental and development test programs for:

DC to DC power converters

DC to AC power inverters

Various electronic and mechanical components for Gemini, Apollo, and Minuteman programs

Inertial switches

Hydraulic components and systems

Other Ordnance Division experience as Lead Test Engineer for XM71 warhead fuze and XM65 training warhead, and as Design Engineer for electronic fuze and timer circuitry

Three years with Bourns, Inc., as phaser and analyzer for military equipment

Seven years in U. S. Navy

Professional Background

BSEE, Iowa State University

Completing MBA, University of Minnesota

J. T. LINGLE, Senior Development Engineer

Experience

Currently assigned in the design and development of solid-state low input voltage power converters, inverters, voltage regulators, transistor circuitry, thermoelectric generators, and mechanical systems.

Project Engineer on low input voltage conversion contract with U. S. Army Engineering Research of Development Laboratory, Contract DA-36-039-SC90808.

Design of three-phase power supply. Includes polyphase input and polyphase output plus several d-c outputs and a-c constant current outputs, using nine transistor regulators (voltage and current).

Specialized in design and development of solid-state power supplies.

Experience dating back to 1952 on applications of transistors, power converters, switching circuits, and voltage regulators.

Active experience on such projects as a 120-watt thermoelectric generator and a transistor switching study of the U. S. Signal Corps

Professional Background

BSEE, University of Minnesota

Registered Professional Engineer, State of Minnesota

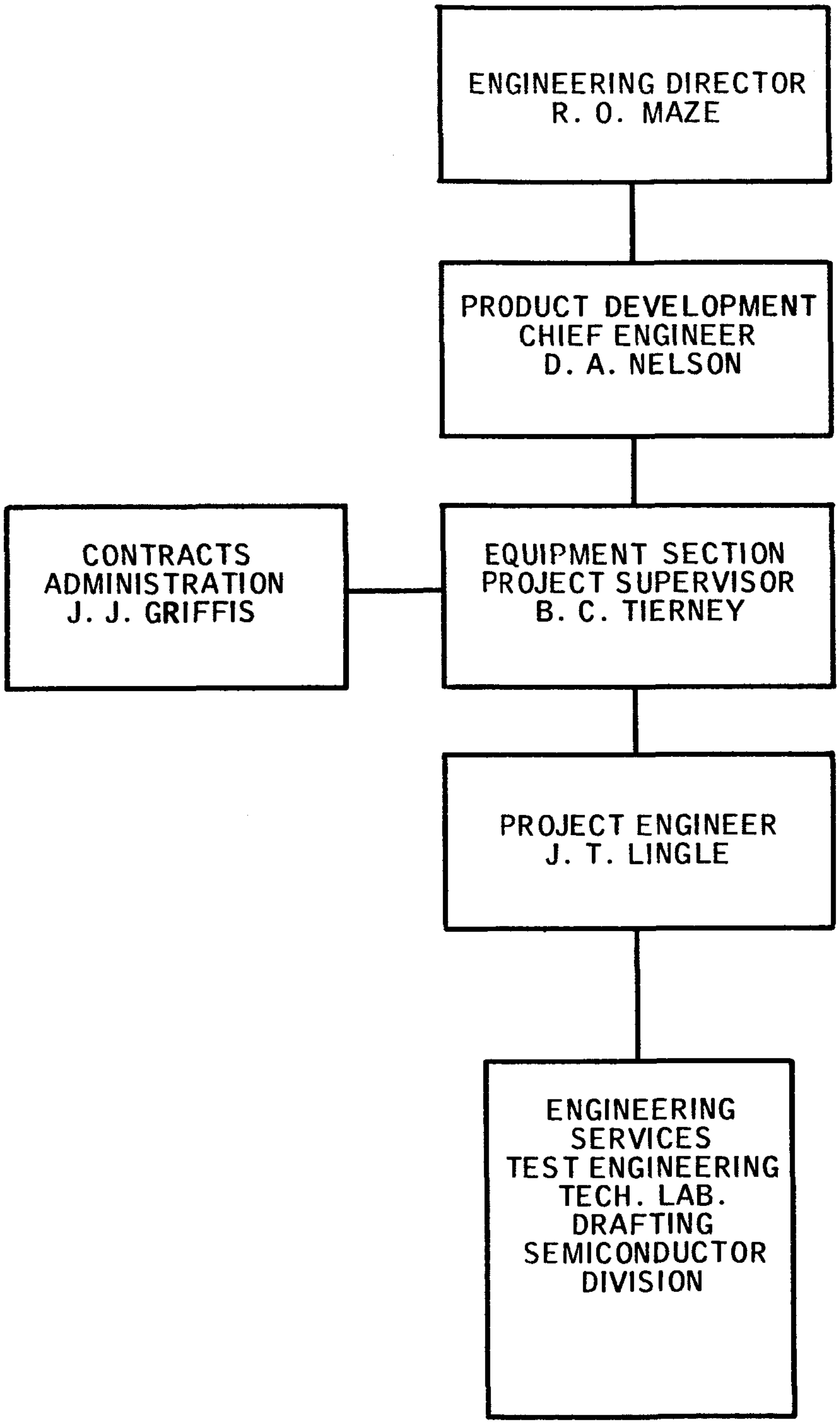

Figure 12 - PROJECT ORGANIZATION CHART

Prepared by John T. Lingle

John T. Lingle

Approved by B C Tierney

B. C. Tierney

D. A. Nelson

D. A. Nelson

APPENDIX "A"

PERFORMANCE DATA FOR A SINGLE CELL FUEL CELL AND LOW INPUT VOLTAGE CONVERTER SYSTEM

APPENDIX "A"

PERFORMANCE DATA FOR A SINGLE CELL FUEL CELL AND LOW INPUT VOLTAGE CONVERTER SYSTEM

To arouse interest in low input voltage converters Honeywell fabricated two low-input voltage converter models to be operated from a single cell fuel cell source. This work was not done under this contract; however, the information obtained regarding converter operation and converter design for operation with fuel cell sources is very applicable to this program. For this reason the information obtained from the converter and fuel cell operating characteristics are included in this report. This fuel cell-converter system information will be a valuable aid in designing the converter for this project.

To illustrate the difference between converter operation from our present laboratory source and from a fuel cell source, the converter operating characteristics utilizing both sources has been included. Performance data for the converter operating from the laboratory-type power source are shown on Figure A-1. This figure shows converter efficiency versus power output for input voltages of . 3 volts to . 9 volts. With the laboratory type power supply the proper input voltage could be maintained and hence higher output powers could be obtained. These curves show that the efficiencies ranged between 75 and 79 per cent over most of the load range for input voltages of . 7 volts or more.

Output powers as high as 70 watts were obtained with the laboratory type power source. Performance data for the converter operating from a fuel cell source is shown on Figure A-2.

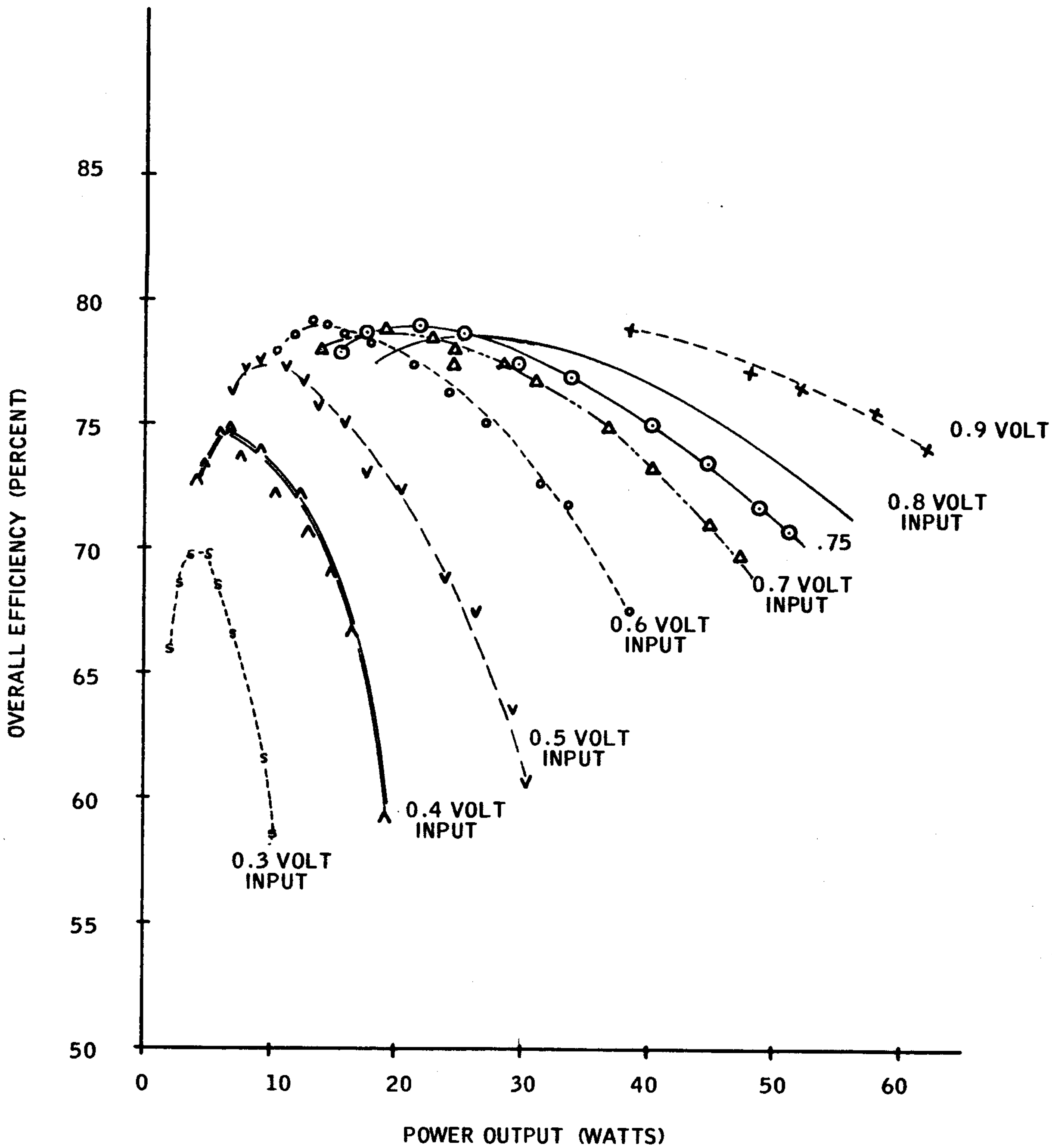

Figure A-1 - PERFORMANCE CURVES FOR A 0.8 VOLT INPUT - 28 VOLT - 30 WATT CONVERTER OPERATING FROM A LABORATORY SUPPLY

The fuel cell terminal voltage at light load was approximately .85 volts. With heavy load the source terminal voltage declined to approximately .7 volts. The curve shows converter efficiency versus converter output while operating from the source voltage, which declined with heavy load. Note that the maximum efficiency was approximately 77 per cent, and it remained nearly constant over the range of 20 to 32 watts output. One reason for the efficiency decline at loads above 32 watts was the source voltage decline at heavy load. The overall efficiency of the converter operating from the fuel cell source was about 3 per cent lower than the efficiency of the same converter operating from the laboratory power supply. The laboratory power supply has a different source impedance which affects efficiency measurements. This power supply had a low a. c. output impedance but also a high d. c. output impedance. The fuel cell on the other hand had a lower d. c. source impedance but probably a higher a. c. source impedance. Input line ripple variations between the two supplies probably contributed to the difference in efficiency readings. The converter operating from the fuel cell may have produced more input line ripple, causing a greater error in the calculated input power which was obtained by multiplication of input voltage and input current meter readings. Because the ripple current tends to lag the ripple voltage, the a. c. component has a power factor which must be considered to obtain correct input power measurements. Therefore, merely multiplying the average d. c. current times the average d. c. voltage will not give the true input power if the ripple is appreciable.

The converter output characteristics when operating from the laboratory type power supply are shown on Figure A-3. Note that these are linear. The output voltage increases with input voltage, and it declines linearly with load. The output characteristics of the converter operating from the fuel cell sources are shown on Figure A-4. The source terminal voltage versus load curves for the laboratory power supply are shown on Figure A-5. The curves indicate that the laboratory type supply has a relatively high d. c. source impedance. To reduce source impedance of the laboratory supply, bleeder resistors have been connected across the source output.

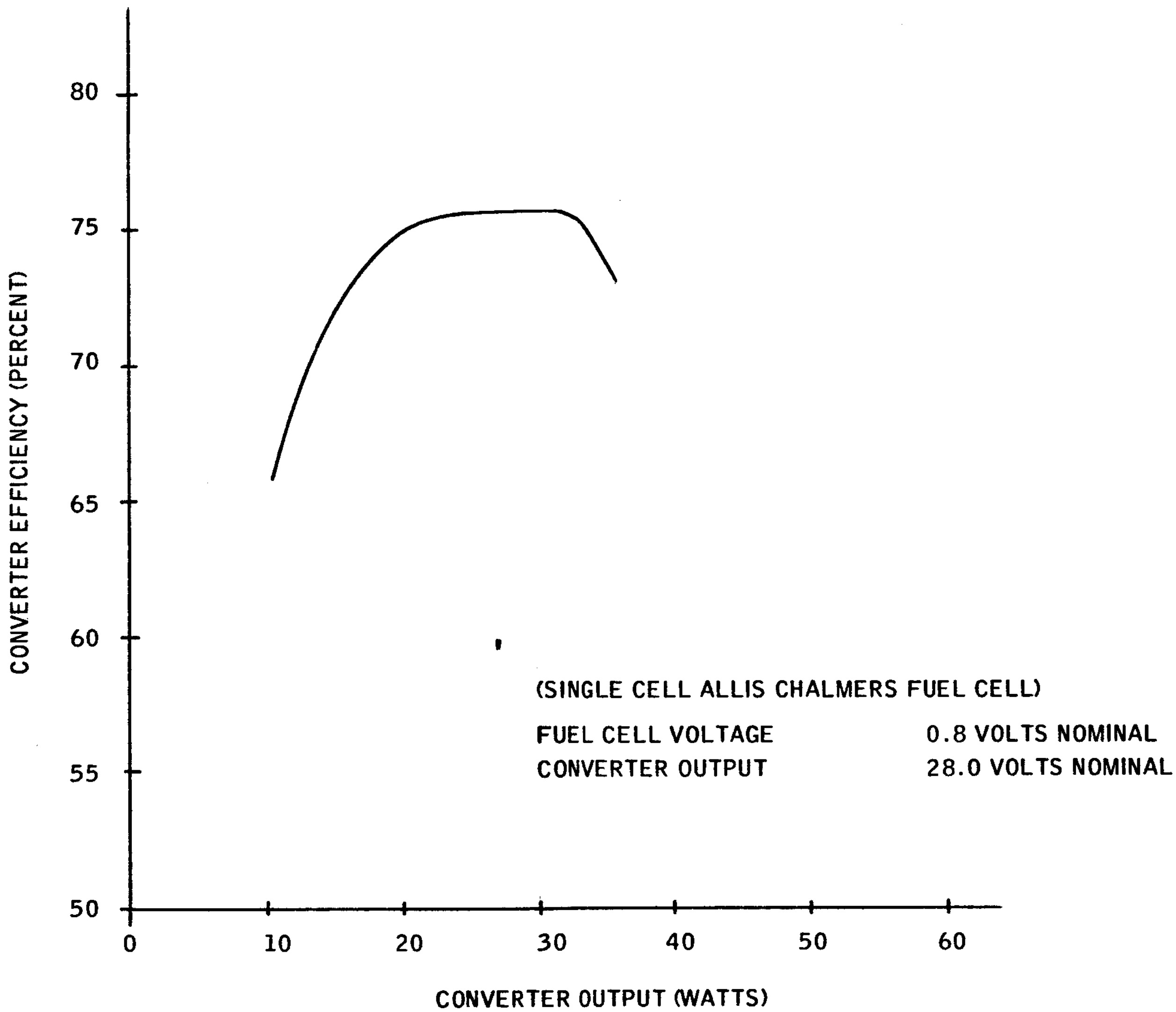

Figure A-2 - OPERATION OF A LOW INPUT VOLTAGE CONVERTER FROM A SINGLE CELL FUEL CELL SOURCE

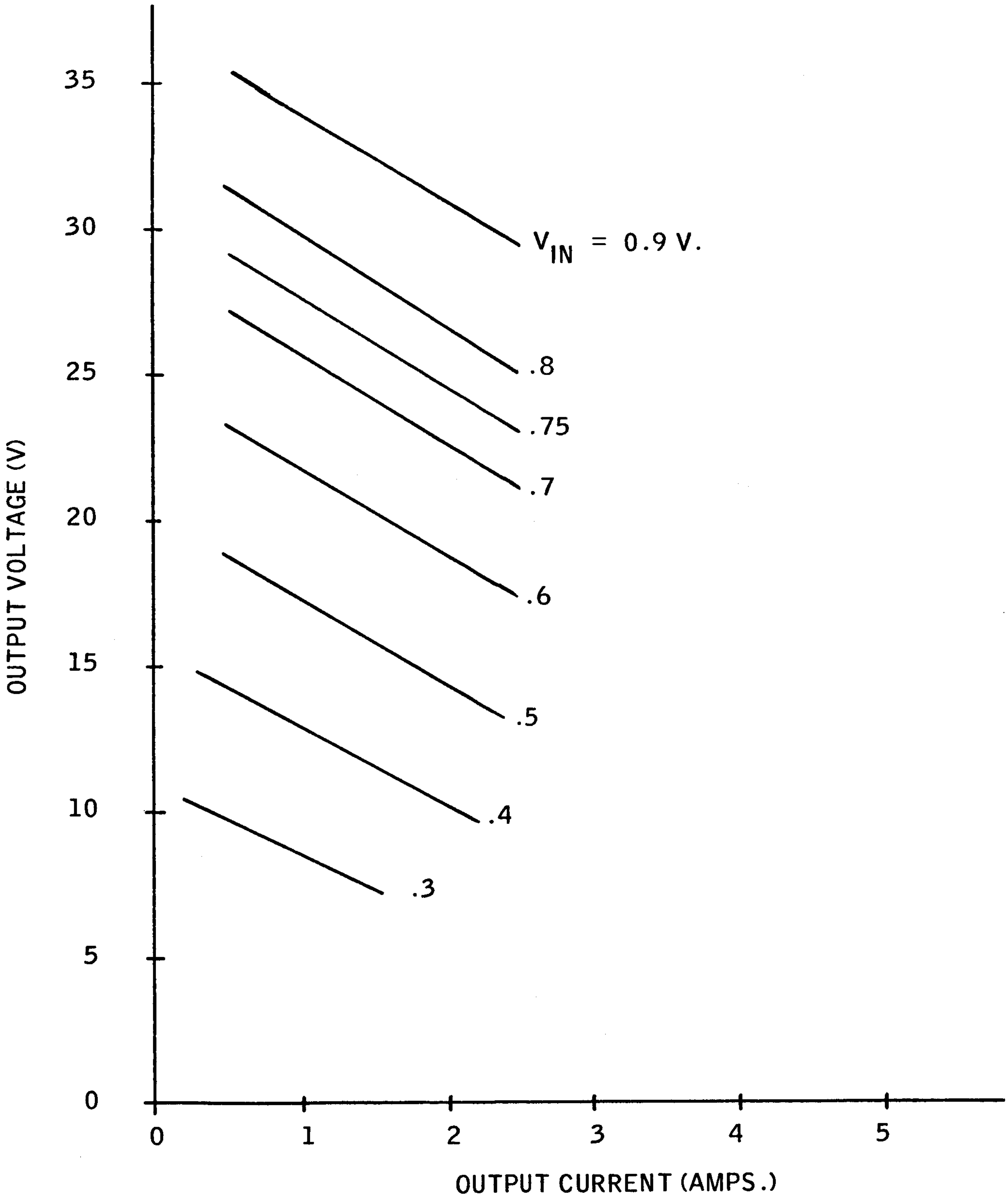

Figure A-3 - CONVERTER OUTPUT CHARACTERISTICS WHEN OPERATING FROM A LABORATORY POWER SUPPLY

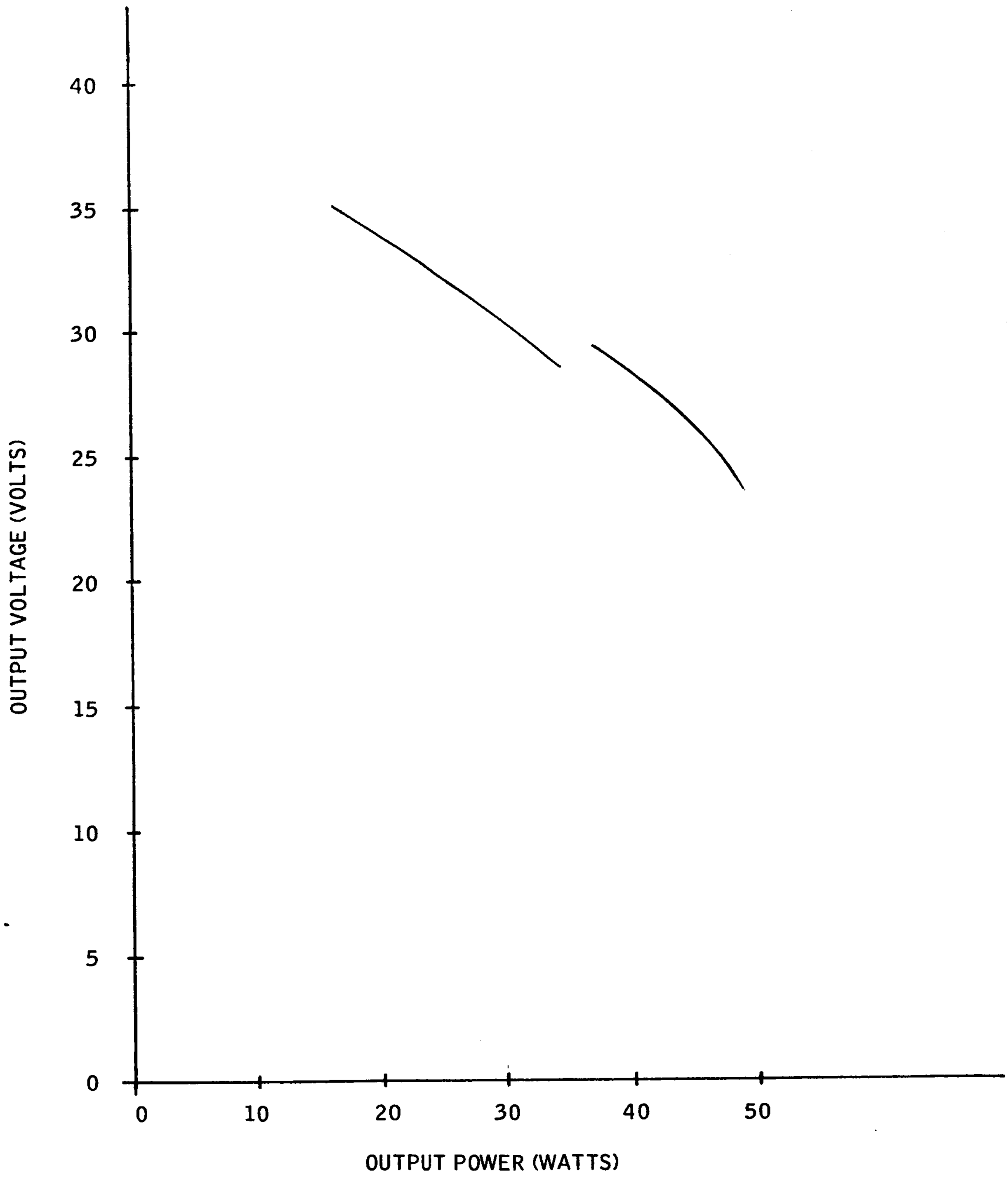

Figure A-4 - FUEL CELL - LOW VOLTAGE CONVERTER SYSTEM OUTPUT CHARACTERISTICS FOR TWO DIFFERENT FUEL CELL OPERATING CONDITIONS

The output terminal voltage versus load for the fuel cell is shown on Figure A-6. This voltage was measured at the ammeter output. Therefore, to obtain the actual fuel cell terminal voltage the ammeter and connecting cable voltage drops must be added to these data. The fuel cell operating conditions (fuel pressure, flow rate, humidity, temperature) were altered when these data were recorded and hence the discontinuity in the curves of Figures A-4 and A-6.

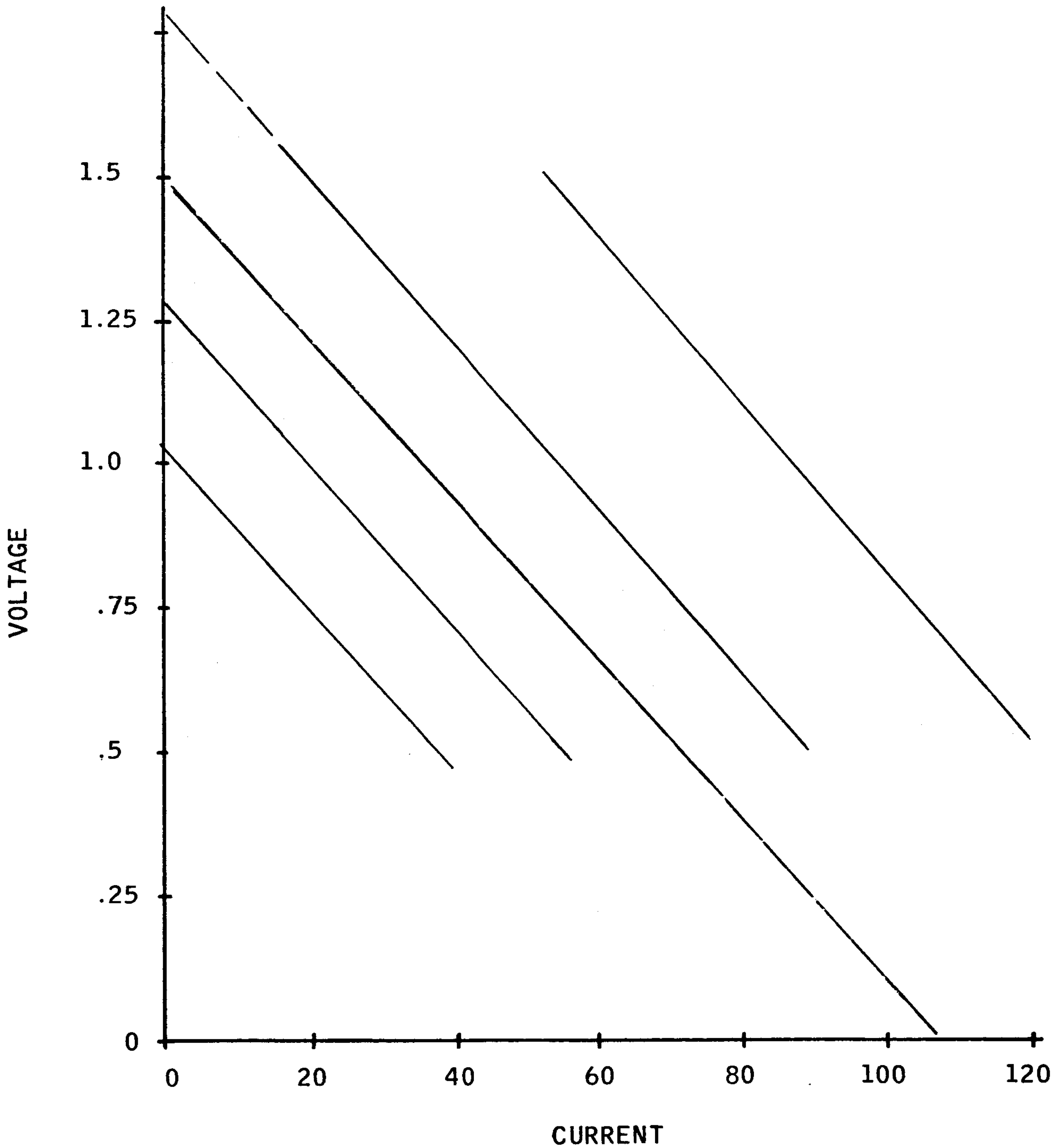

Figure A-5 - LABORATORY POWER SUPPLY CHARACTERISTICS FOR VARIOUS SET POINTS

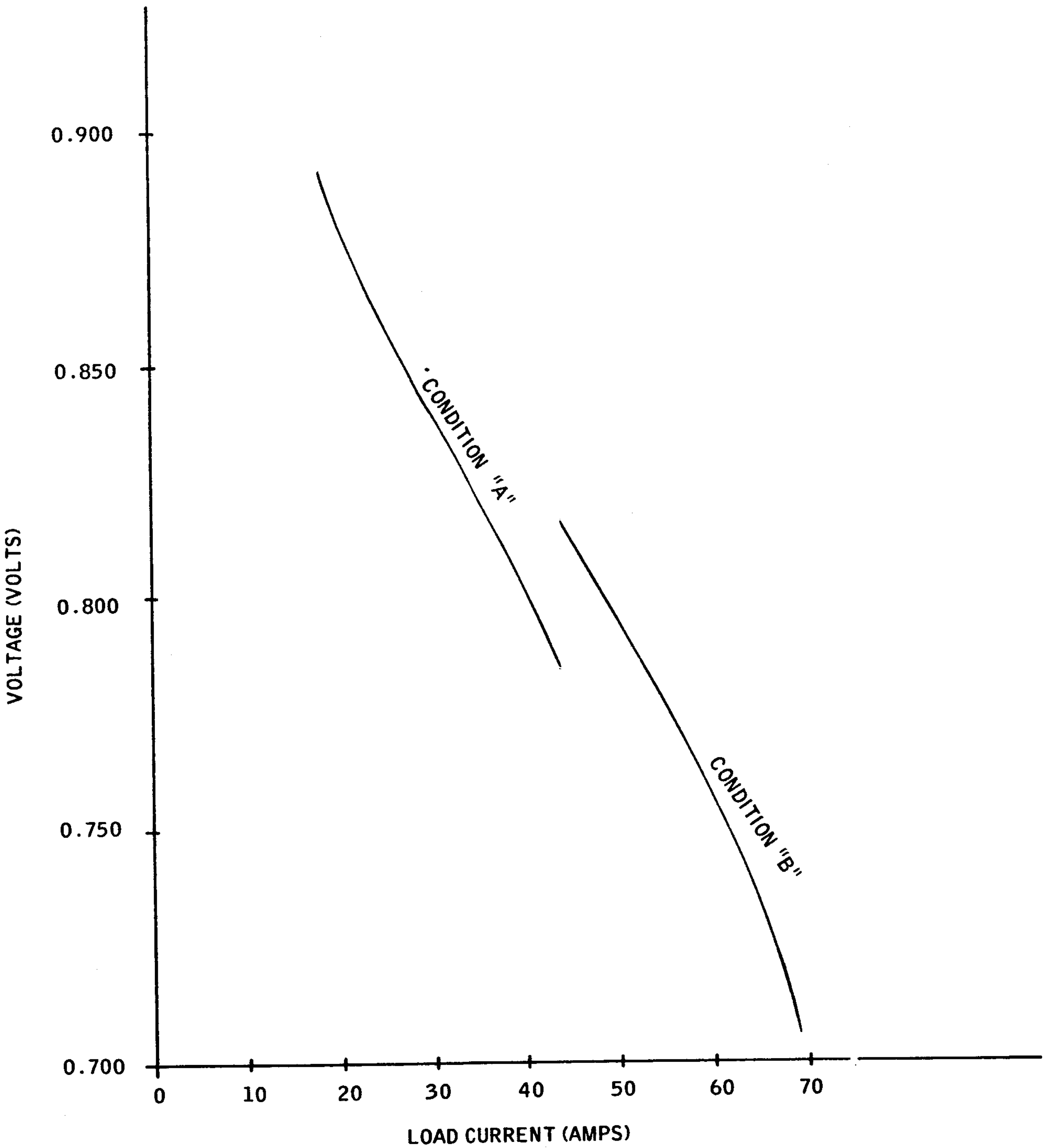

Figure A-6 - FUEL CELL OUTPUT VOLTAGE VERSUS LOAD CURRENT FOR TWO DIFFERENT FUEL CELL OPERATING CONDITIONS